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Pixel design and Characterization of High-performance tandem OLED Microdisplays

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To my parents

不聞不若聞之，聞之不若見之，見之不若知之，知之不若行之；學至於行之而止矣。

What I hear I forget, what I see I remember, what I do I understand; true learning continues up to a point that action comes forth.

荀子《儒效篇》

Xunzi (340 – 245 BC)

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Abstract

Organic Light-Emitting Diode (OLED) microdisplays - miniature Electronic Displays comprising a sandwich of organic light emitting diode over a substrate containing CMOS circuits designed to function as an active matrix backplane – were first reported in the 1990s and, since then, have advanced to the mainstream. The smaller dimensions and higher performance of CMOS circuit elements compared to that of equivalent thin film transistors implemented in technologies for large OLED display panels offer a distinct advantage for ultra-miniature display screens. Conventional OLED has suffered from lifetime degradation at high brightness and high current density. Recently, tandem-structure OLED devices have been developed using charge generation layers to implement two or more OLED units in a single stack. They can achieve higher brightness at a given current density. The combination of emissive-nature, fast response, medium to high luminance, low power consumption and appropriate lifetime makes OLED a favoured candidate for near-to-eye systems. However, it is also challenging to evaluate the pixel level optical response of OLED microdisplays as the pixel pitch is extremely small and relative low light output per pixel. Advanced CMOS Single Photon Avalanche Diode (SPAD) technology is progressing rapidly and is being deployed in a wide range of applications. It is also suggested as a replacement for photomultiplier tube (PMT) for photonic experiments that require high sensitivity. CMOS SPAD is a potential tool for better and cheaper display optical characterizations.

In order to incorporate the novel tandem structure OLED within the computer aided design (CAD) flow of microdisplays, we have developed an equivalent circuit model that accurately describes the tandem OLED electrical characteristics. Specifically, new analogue pulse width modulation (PWM) pixel circuit designs have been implemented and fabricated in small arrays for test and characterization purposes. We report on the design and characterization of these novel pixel drive circuits for OLED microdisplays. Our drive circuits are designed to allow a state-of-the-art sub-pixel pitch of around 5 μm and implemented in 130 nm CMOS. A performance comparison with a previous published analogue PWM pixel is reported. Moreover, we have employed CMOS SPAD sensors to perform detailed optical measurements on the OLED microdisplay pixels at very high sampling rate (50 kHz, 10 μs exposure), very low light level (2×10^{-4} cd/m^2) and over a very wide dynamic range (83 dB) of luminance. This offers a clear demonstration of the potential of the CMOS SPAD technology to reveal hitherto obscure details of the optical characteristics of individual and groups of OLED pixels and thereby in display metrology in general.

In summary, there are three key contributions to knowledge reported in this thesis. The first is a new equivalent circuit model specifically for tandem structure OLED. The model is verified to provide accurately illustrate the electrical response of the tandem OLED with different materials. The second is the novel analogue PWM pixel achieve a 5μm sub-pixel pitch with 2.4 % pixel-to-pixel variation. The third is the new application and successful characterization experiment of OLED microdisplay pixels with SPAD sensors. It revealed the OLED pixel overshoot behaviour with a QIS SPAD sensor.

Lay summary

This thesis aims at the exploration of the development of high-performance tandem structure OLED (TOLED) microdisplay pixel and its characterization. The pixel design is targeting to deliver high dynamic range to drive the TOLED which is expected with a doubled current efficiency. In the meanwhile, the pixel is required to have a small pixel pitch, minimal connectivity and low power consumption to be integrated on a scalable microdisplay pixel array.

The first challenge is the development of a SPICE model which offers high accuracy simulation to the TOLED electrical response. A dual loop model is developed which emulates the stacked structure of a TOLED. The model is verified over fitting of multiple TOLED samples with the same material to illustrate the OLED manufacturing process variation. Moreover, it is also employed for parameter extraction of multiple TOLEDs with different OLED layer materials to investigate the effect of different materials on the electrical characteristics.

TOLED has doubled current efficiency compared to the conventional single-unit OLEDs. However, the high current efficiency comes at a price of a doubled drive voltage. The microdisplay pixel needs to drive a high voltage output and high dynamic range. To address these challenges, several microdisplay pixels are designed and implemented. An annular shape MOSFET is employed to demonstrate low leakage and high input signal dynamic range pixels. In addition, an analogue PWM pixel is designed. The pixel achieved the pulse-width in-pixel generation without any bias current at a sub-pixel pitch of 5×5 μm^2. It allows a full dynamic range (0 to VDD) for the drive of the TOLED anode node. The analogue pixel realises 2.3% variation for 1000 Monte Carlo simulations and less than 1% linearity and 2% variation in a 4×12 test array for electrical measurement. Finally, optical characterization of the TOLEDs pixels is explored. SPAD sensors are optimum for high sensitivity and high time resolution measurements. Nonetheless, for the field of CMOS SPAD sensors, much remains to be done. It is worthwhile to investigate the feasibility of using CMOS SPAD sensors for display metrology, and whether in some cases, they can outperform the current luminance sensors.

Declaration of Originality

I hereby declare that the research recorded in this thesis (excluding the exceptions stated below) and the thesis itself originated with and was composed by myself.

Other people who have contributed to this work are acknowledged and / or referenced appropriately within.

This work has not been submitted for any other degree or professional qualification except as specified.

Hanning Mai

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Publications

- List of publications with primary contributions from the author in chronological order:

[1] H. Mai and I. Underwood, "Characterization and Modelling of Tandem structure OLED," in SID-ME Chapter Spring Meeting 2017, 2017.

[2] H. Mai, R. Henderson, and I. Underwood, "Pixel Drive Circuit Design for AMOLED Microdisplays," in Eurodisplay, Berlin, 2017, vol. 1, no. 1, pp. 32-33.

[3] H. Mai, I. Gyongy, N. A. Dutton, R. K. Henderson, and I. Underwood, "16-2: Distinguished Student Paper: Characterization of Electronic Displays using Advanced CMOS Single Photon Avalanche Diode Image Sensors," in SID Symposium Digest of Technical Papers, 2018, vol. 49, no. 1, pp. 181-184: Wiley Online Library. https://doi.org/10.1002/sdtp.12514

[4] H. Mai, I. Gyongy, N. A. Dutton, R. K. Henderson, and I. Underwood, "Characterization of electronic displays using CMOS single-photon avalanche diode image sensors," Journal of the Society for Information Display. https://doi.org/10.1002/jsid.661

[5] I. Underwood, H. Mai, T. A. Abbas, I. Gyongy, N. A. W. Dutton, and R. Henderson, "Invited Paper - Single-Photon-Capable Detector Arrays in CMOS: Exploring a New Tool for Display Metrology," in International Conference on Display Technology 2018, Guangzhou, China, 2018.

Acronyms

AMOLED	active matrix OLED
ADC	analogue-to-digital converter
ATC	analogue to time converter
AR	augmented reality
APD	avalanche photodiodes
BSI	back side illuminated
CRT	cathode ray tube
CCD	charge-coupled device
CGL	charge-generation layer
CMOS	complementary metal oxide semiconductor
CAD	computer aided design
DCR	dark count rate
DOS	density of states
DMD	digital micromirror devices
dSiPM	digital silicon photomultiplier
DAC	digital-to-analogue converter
EL	electroluminescent
EBL	electron blocking layer
EIL	electron injection layer
ETL	electron transport layer
ECDM	extended correlated disorder model
EGDM	extended Gaussian disorder model
FOV	field of view

FLIM	fluorescence lifetime imaging microscopy
FN	Fowler-Nordheim
GDM	Gaussian disorder model
HMD	head mounted display
HOMO	highest occupied molecular orbital
HBL	hole blocking layer
HIL	hole injection layer
HTL	hole transport layer
ITO	indium-tin-oxide
IC	integrated circuit
LCoS	liquid crystal on silicon
LC	liquid crystal
LVDS	low voltage differential signaling
LUMO	lowest unoccupied molecular orbital
MiM	metal insulator metal
MOM	metal-oxide-metal
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
MED	MicroEmissive Displays
µLED	micro-LED
MC	Monte Carlo
MG	Mott-Gurney
MS	Mott-Shockley
NTE	near-to-eye

ND	neutral density
OLED	organic light-emitting diode
PIN-OLED	P-doped layer, Intrinsic layer, N-doped layer OLED
PMT	photomultiplier tube
PDE	photon detection efficiency
PDP	photon detection probability
PDP	plasma panel display
POLED	polymer OLED
PF	Poole-Frenkel
PWM	pulse width modulation
PCM	pulse-coded modulation
QIS	quantum image sensor
QVGA	quarter video graphics array
ROI	region of interest
RS	Richardson-Schottky
SNR	signal-to-noise ratio
SPICE	Simulation Program with Integrated Circuit Emphasis
SPAD	single photon avalanche diode
SMOLED	small molecule OLED
SCLC	space charge limited current
SLM	spatial light modulators
SRAM	static random-access memory
SXGA	super extended graphics array
TOLED	tandem OLED

TCAD	technology computer aided design
3D	three-dimensional
VTH	threshold voltage
TCLC	trap-charge limited current
VR	virtual reality

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1 Introduction

This thesis explores the design of microdisplays based on complementary metal oxide semiconductor (CMOS) active matrix backplane and tandem structure organic light-emitting diode (OLED) technology. OLED has a distinctive characteristic of self-emissive. Tandem or stacked structure OLED offers improved current efficiency and lifetime. Combining both of these, the application of tandem OLED (TOLED) in microdisplay yields a microdisplay with extremely high contrast ratio, low power consumption and fast switching. Moreover, for the same reason, it is difficult to characterise a TOLED microdisplay.

1.1 OLED microdisplay

OLED technology was first reported in the late 1990s and has since begun to challenge liquid crystal (LC) in commercial display applications. Over the years, they have impacted each other in research and development. Research has continued improving LC, as a light modulation device, towards fast switching, wide viewing angle and good colour performance with LED backlights. Research of OLED has been focused on the efficiency, lifetime and low-cost manufacturing process. OLED, as a slightly younger technology, has gained market share from LC in the general applications, such as TV, mobile phone screens etc. However, the competition will continue at least for the near future.

The term microdisplay refers to an ultra-miniature display integrated on a smart silicon chip, designed to be viewed under optical magnification. There are mainly two classes of microdisplays, modulating and emissive. Modulating microdisplays include digital micromirror devices (DMD) and LC on silicon (LCoS). Emissive microdisplay is mostly based on OLED technology except for micro-led which is gaining momentum over the last years. For the advantages of low power consumption and high contrast ratio, OLED is preferred over LC and DMD, in terms of the "near-to-eye" (NTE) application. However, there are still issues like brightness, reliability, lifetime, scalability and the manufacturing cost that need to be resolved.

1.1.1 Historical microdisplay design overview

The development of microdisplays based on MOS backplane can be dated back to the 1970s relating to a class of devices known as spatial light modulators (SLM) or light valves. The first demonstration of MOS active matrix SLM is based on nematic liquid crystal developed by Ernstoff et al. [1] The pixel circuit is as simple as a sample and hold circuit which consists a single MOSFET switch and a capacitor. As the CMOS technology in that era is limited, most of the reported LCoS pixels employ a single bit dynamic memory [1-3] or static memory [4]. Later, Underwood et al. employed a MOS bi-stable flip-flop memory (SRAM) with an XNOR gate pixel [5] which opened a new door for a fully digital driving method. More recently, the advanced CMOS technology with small process node has allowed the

implementation of complex pixel circuits to improve the LCoS performance, such as in-pixel analogue comparator [6], multi-bit DRAM [7] and multi-bit SRAM [8].

The other main type of CMOS microdisplay that followed LCoS SLM is the DMD which was developed by Hornbeck et al.[9, 10] The two electrodes of a DMD pixel are driven by a high voltage in-pixel SRAM cell [11-13]. Both high voltage and low voltage CMOS MOSFETs are required in pixel: the low voltage MOSFETs allow high bandwidth row/column driver interface; the high voltage SRAM cell is used to apply a large electric field on the DMD.

1.1.2 OLED microdisplay survey

The history of the development of an OLED microdisplay can be dated back to 1990s. Several research groups have reported the possibility of OLED integrated on a CMOS substrate with both small-molecule type [14] and polymer type [15]. The initial design of OLED microdisplay pixel circuit referred to are the TFT-based OLED displays [16, 17] which have been available for a longer duration. The OLED microdisplay pixel circuit can be classified into several types, such as digital or analogue domain, voltage or current drive. In addition, the compensation of V_T (threshold voltage) and mobility of the drive transistor is applied to the pixels mentioned above circuits to enhance luminance uniformity. The compensation scheme is more popular for TFT displays which suffer from more serious mismatch than CMOS microdisplays. An example V_T and mobility compensation pixel for CMOS microdisplays is described in section 3.4.2.2.

One of the pioneers is eMagin Corporation (eMagin), who started the development of CMOS OLED microdisplay in 1995. IBM and eMagin presented the first OLED on crystalline silicon display applied for a wristwatch [18]. However, it is more of a direct view display than a microdisplay. eMagin showed the first OLED microdisplay demonstration, an SXGA (1280×1024, monochrome) device, at the SID Display Week 2000[1] [19]. About the same time, a research group in Agilent Technologies Inc. developed an XGA polymer OLED microdisplay [20]. It employed an analogue PWM pixel driver backplane designed by Blalock et al. [6], which was initially designed for LCoS microdisplay. Later, in 2004, Underwood et al. from MicroEmissive Displays (MED) demonstrated the first polymer OLED microdisplay as a commercial product [21], which is recognized as 'the world's smallest color TV screen' [22].

In recent years, the development of OLED microdisplay devices has made substantial progress thanks to the industrial interest. Sony, who has already been developing AMOLED displays since the 2000s [23, 24], published their first OLED microdisplay in 2012 [25, 26]. MicroOLED, a spin-out company from CEA-Leti in 2007, has presented an SXGA (1280×1024) OLED microdisplay [27] in 2012. Other display companies such as Kopin [28], Olightek [29] have also revealed their OLED microdisplay devices recently. Apart from traditional OLED microdisplays, Fraunhofer FEP developed a

[1] The display of the year gold award winner

revolutionary bidirectional microdisplay in 2011 which is beneficial for eye-tracking for HMDs (head mounted displays).

Figure 1-1 shows the evolution of OLED microdisplay pixel size and definition from 2001 [19, 21, 26, 27, 30-50]. As shown in Figure 1-1 (a), the subpixel size decreases over the years as the use of more advanced CMOS process (from 0.35µm [30, 31] to 0.18µm [33, 41, 49]) and improvement in OLED and colour filter processing [44, 49]. Nevertheless, the slope of the decreasing trend has decelerated since 2012. It is difficult to shrink the pixel size further to less than 30 μm^2. The OLED device is usually driven by a high voltage (5V to 10V). Although the in-pixel storage can be low voltage (<1.2V), it requires a relatively high voltage (3.5~5V) driver for the OLED. The drive MOSFETs need to be thick oxide MOSFETs which do not scale as the CMOS process. Moreover, there hasn't been any microdisplay that employs CMOS process <130nm scale.

The evolution of the number of pixels of a microdisplay is shown in Figure 1-1 (b). The resolution of OLED microdisplay devices has advanced from QVGA monochrome [31] to 2K × 2K 24-bit colour [44]. Moore's law has been a beneficiary to the development of large microdisplay backplane, giving lower power consumption of the digital peripheral drivers and the smaller cost of manufacture. However, the high number of pixel count cause difficulties to the design on a system level. For example, more than 12 Gbps (Gigabit per second) data need to be processed and transmitted through low voltage differential signalling (LVDS) data channels in the 2K × 2K design presented by eMagin.

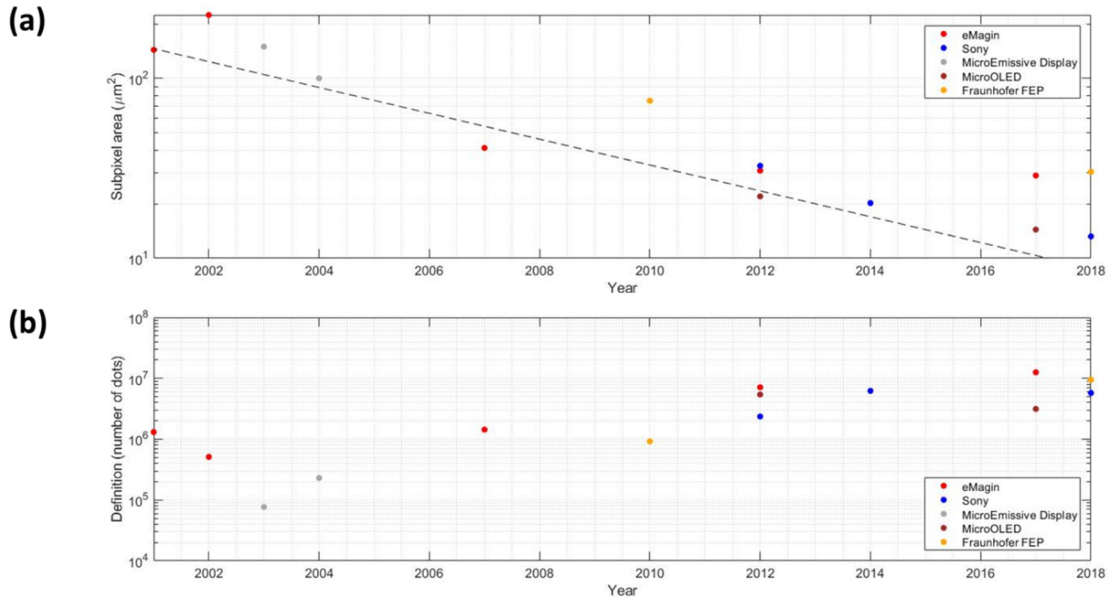


Figure 1-1 OLED microdisplay (a) sub-pixel pitch[2] and the fitted Moore's law trend of decreasing pixel pitch versus time (b) display resolution advancement over years (data collected from [19, 21, 26, 27, 30-50])

[2] Some devices such as [46-48] are with different subpixel size for RGB configuration. For the purpose of comparison, the subpixel size is the pixel size divided by number of subpixels.

1.2 Tandem OLED

Since the first demonstration of small molecule OLED (SMOLED) by Tang and VanSlyke in 1987 [51] and of the polymer OLED (POLED) by Burroughes et al. in 1990 [52], OLEDs can be classified by the type of organic material used. Apart from SMOLED and POLED, in the late 1990s, Baldo, Forrest and Thompson made a breakthrough in improving the quantum efficiency (≥90%) of the OLED devices with phosphorescent light-emitting materials [53]. More recently, more sophisticated OLEDs have been developed with a structure of multiple organic layers sandwiched between the anode and the cathode. For example, the structure of a small molecule P-doped layer, Intrinsic layer, N-doped layer (PIN) OLED is shown in Figure 1-2. It consists of hole injection layer (HIL), hole transport layer (HTL), electron blocking layer (EBL), hole blocking layer (HBL), electron transport layer (ETL), electron injection layer (EIL) and RGB emitting layers. The emitters of a high-efficient OLED device usually consist of phosphorescent dopant. The classification of OLED based on the material is blurred, as a PIN-OLED can stack different types of organic layers and phosphorescent dopants.

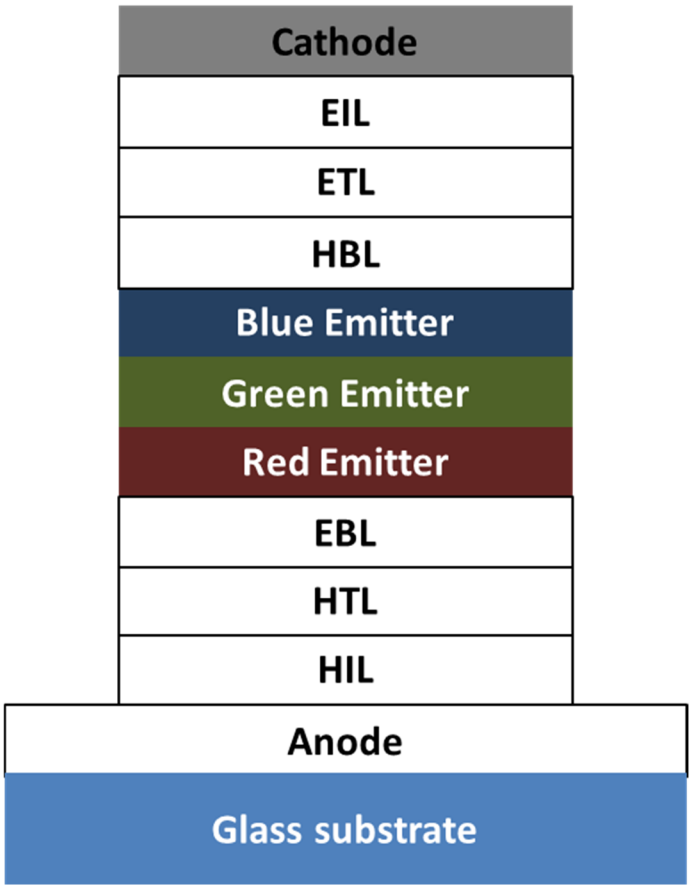


Figure 1-2 High-efficiency PIN OLED device structure [54]

Tandem (or staked) structure OLED was introduced in order to improve the lifetime at high brightness. The TOLED is developed by depositing more than one organic emissive layers in a vertical stack with

a charge-generation layer (CGL) in between. By stacking N electroluminescent (EL) units, the theoretical maximum luminance level will be N-fold for the same current density. The lower current level avoids severe OLED degradation. The CGL is critical for the OLED performance in terms of efficiency and luminance. An example of tandem OLED device structure is shown in Figure 1-3.

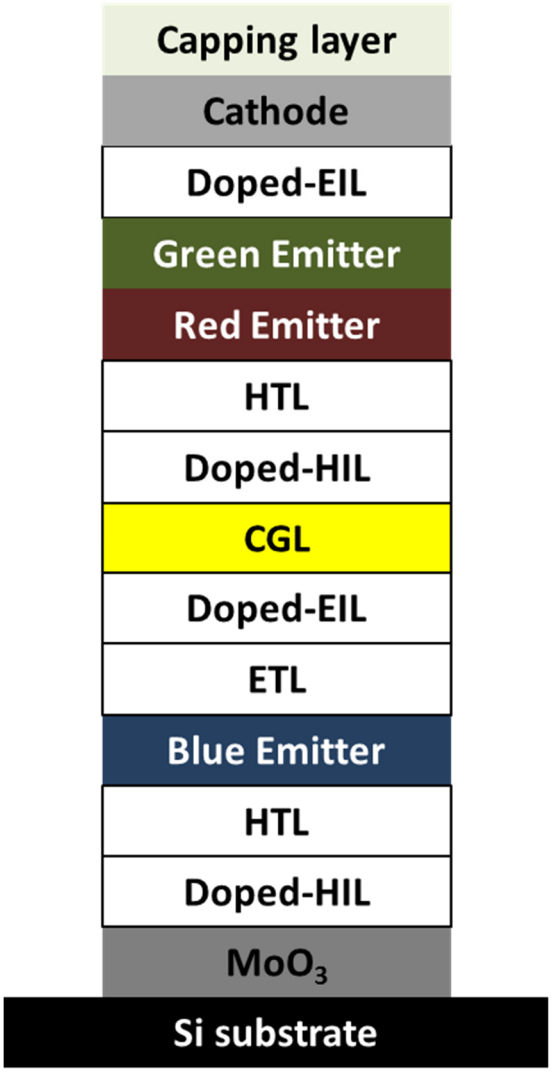


Figure 1-3 Tandem OLED device structure

The first reported TOLED, which used a CGL to two emitting layers, was developed by Kido et al. [55] in 2003. After that, intensive research and development effort have been undertaken in the field of TOLED. TOLED has been shown to be promising for high brightness [56-58] without sacrificing the OLED lifetime. Therefore, displays that employ TOLED are robust against ageing-induced image sticking and burn-in in OLED displays.

1.3 OLED microdisplay characterisation and SPAD technology

Improvement in OLED microdisplays is leading towards fast switching, high contrast ratio and small pixel pitch. In order to measure and quantify the optical characteristics, these improvements require the light measurement devices to have a high sampling rate, high dynamic range and low signal to noise ratio. Unlike other conventional display applications (such as mobile phones, TVs), it is difficult to evaluate the pixel level optical performance of an OLED microdisplay. OLED microdisplay pixels are tiny, usually smaller than 10 µm pitch, often with a low total light output per pixel. Moreover, the optical switching time of an OLED can be much less than one microsecond **[59]**.

The single photon avalanche diode (SPAD) is a specially designed avalanche photo-diode based device. The avalanche photo-diode is biased above the breakdown voltage to operate in Geiger mode, allowing single photon detection. Combining the features of single photon sensitivity and picosecond temporal resolution, SPAD sensors are potential to capture images with extremely high sensitivity in both optical and temporal domains. The first CMOS SPAD was reported in 2003 [60], by Rochas et al. Since then, there has been growing interest in CMOS SPAD sensors for their potential to outperform the traditional CCD and CMOS based technologies in capturing single photons with picosecond resolution.

SPADs and SPAD arrays have addressed a wide range of applications due to their impressive performance capabilities - very fast response (dead time in the order of nanoseconds[61]), extremely high frame rate, higher than one mega frame per second (fps), single-photon sensitivity and ability to time-stamp the instant of photon capture. CMOS SPAD offers the possibility to develop dense arrays of SPAD pixels with local (in-pixel) circuitry also with sophisticated on-chip signal conditioning and processing [60] that can be custom-designed and thus optimised for any given application. For example, recently reported applications of SPADs and SPAD arrays have ranged from time-of-flight three-dimensional (3D) vision [62] and fluorescence lifetime imaging microscopy (FLIM) [63] to imaging of ultrafast physical processes like light-in-flight [64]. The market potential of CMOS-SPADs has grown to the point that many CMOS foundries have developed advanced CMOS processes that are optimised for both CMOS circuits and SPAD detectors, see for example [65]. With the recent development of these SPAD-optimised advanced CMOS processes, it is becoming possible to overcome some of the limitations of earlier generations of CMOS-SPAD arrays such as low Fill-Factor and implement high-sensitivity SPAD quantum image sensor (QIS) arrays.

1.4 Research Aims and Background

This research project was carried out as part of the Pilot Optical Line for Imaging and Sensing (POLIS, http://polis.minalogic.net/, Project ID 621200), work package 3 (WP3), under the funding scheme Joint Technology Initiatives - Collaborative Project (ENIAC), FP7. POLIS is a multi-discipline project, aiming at furthering the innovation capability of CMOS image and optical sensors. The POLIS WP3 targets offering low power consumption and low-cost OLED-on-silicon micro-displays for augmented

reality (AR) applications, e.g. vision aids for visually impaired people, AR information in the field of logistics or maintenance. A very high luminance of 3000 to 5000 cd/m^2 is required for these see-through applications.

The core solution of POLIS WP3 is the development of novel OLED stack for direct colour generation and tandem structure for high efficiency. While the central theme of the POLIS WP3 revolves around the development of novel high luminance OLED stacks, this work focuses on investigating the pixel design and evaluating the pixel performance for a TOLED microdisplay.

The main aim was to create a compact and scalable pixel design for TOLED. The first task is to develop an accurate SPICE model of the novel TOLED for the purposes of pixel circuit design and simulations. As TOLED is yet to be applied for commercial display, most of the OLED modelling work is focused on conventional PIN-OLED. However, a clear difference is observed for the electrical characteristics (current density – voltage) of single – unit OLED and TOLED with similar material [66]. Further understanding and modification of the conventional single – unit OLED model are required.

The starting point of the pixel circuit design is the conventional 2-NMOSFET pixel, with one transistor as a switch and the other as a source follower. Although the pixel is compact to implement in small pixel pitch, its dynamic range is limited for driving TOLED. As the microdisplay pixel is small, the pixel functionality is constraint by the pixel area. The primary aim is to develop a proof-of-concept high dynamic range TOLED pixel with small pixel pitch.

Finally, optical characterisation of TOLED pixels is explored. SPAD sensors are optimum for high sensitivity and high time resolution measurements. Nonetheless, for the field of CMOS SPAD sensors, much remains to be done. It is worthwhile to investigate feasibility if using CMOS SPAD sensors for display metrology, and whether in some cases, they can outperform current luminance sensors.

1.5 Thesis

Chapter 2 of this thesis details the development of a SPICE model for TOLED. A literature review of OLED, its operation principles, and devices physics is presented. Different electrical models for OLEDs are reviewed and discussed. The detailed measurement and modelling of a single-unit OLED and a TOLED will be provided. There will also be a discussion of the effect of different CGL and ETL on the electrical characteristics of TOLEDs.

Based on the TOLED SPICE model developed in Chapter 2, Chapter 3 presents several pixel circuits for TOLED microdisplays. The conventional 2T pixel and the use of an annular layout transistor is discussed. A novel 6T analogue PWM pixel and couple variations of it are presented. Several test arrays of the pixel circuit designs are fabricated in 130nm process. White TOLED stack is deposited on the test pixel arrays. The characterisation results are presented with its scalability and limitations of such pixels.

Chapter 4 introduces an application of CMOS SPAD sensors for optical measurements of OLED microdisplay pixels. High dynamic range and high sampling rate measurements are demonstrated by using the reconfigurable test arrays described in Chapter 3. The feasibility of CMOS SPAD sensors for electronic display characterisation is discussed. The implications of high sensitivity and high time resolution of the SPAD sensors are highlighted.

In Chapter 5, the conclusions from this research are presented. The outlook for future OLED microdisplay and high-speed CMOS SPAD sensor for display metrology application are discussed.

2 Tandem OLED characterisation and modelling

2.1 Introduction

For an active matrix OLED (AMOLED) display driver circuit, a signal (either voltage or current) is generated to drive each OLED subpixel. The amplitude of this signal controls the luminance. Knowledge of the electrical load of the OLED is required to optimise the AMOLED drive circuit. A model that accurately describes the OLED electrical characteristics is usually developed to facilitate accurate circuit simulation.

With the recent progress in tandem structure OLED research, it starts to draw attention to the display applications of TOLEDs [67-69]. An accurate behavioural model is required in order to design and test active matrix OLED (AMOLED) displays. Modelling of single-unit OLEDs electrical response has been discussed in the previous literature. Some studies have investigated the modelling of the carriers transport and the energy bands inside OLEDs [70, 71]. Other approach is to develop equivalent circuit SPICE models [72-75]. The models are built with standard SPICE components. Each SPICE component composing the circuit is described by an equation similar to model equations associated with a physical mechanism like the injection of charges or space charge controlled conduction. These models are preferred for their compatibility with commercial integrated circuit (IC) design tools, e.g. Cadence Design Suite.

The modelling of single-unit OLED is quite mature for both energy band levels and SPICE models. There are some differences between the single-unit OLED and TOLED. Previous models cannot emulate the full electrical characteristics of TOLEDs.

In this chapter, we will first give an overview of the conduction theories based on organic semiconductor physic. Measurement and characterisation of both conventional single EL OLED and TOLED will be discussed. We will focus on the electrical response rather than the detail physical transport phenomena within each organic layer. We will provide a novel SPICE model for tandem structure OLEDs.

2.2 Device physics of OLEDs

2.2.1 Disordered energy states in OLEDs

For the two classes of organic semiconductors, small molecules and polymers, they both have a π-conjugated molecular transport system. In these conjugated molecules, a π-orbital is formed out of the plane of sp^2 in which the C-C, C-H bonds, and σ-bonds reside. A hole or an electron in these orbitals does not belong to a particular atom. These charge carriers are transported through hopping instead of ballistic motion in between the conjugated molecules.

In amorphous semiconductors like small conjugated molecules and polymers, the energy states are disordered. There are no distinct energy bands to model charge transport. Instead of the valence band

and the conduction band of the π-conjugated system form the occupied molecular orbitals and unoccupied molecular orbital. The highest occupied orbitals and lowest unoccupied orbitals are usually referred to as HOMOand LUMO, respectively. When a photon is absorbed with energy higher than E_g, the energy gap between HOMO and LUMO, an excited electron will jump to the LUMO, with a hole generated in the HOMO. On the other hand, when an electron in LUMO recombines with a localised (in short distance) hole in the HOMO, a bound exciton is formed. Since the hole and electron are now bound by a Coulomb attraction radiative decay of the exciton result in a photon with energy E_{hv}, lower than E_g. Figure 2-1 shows the representation of Energy structure of such an organic semiconductor, and the process of recombination of an electron-hole pair.

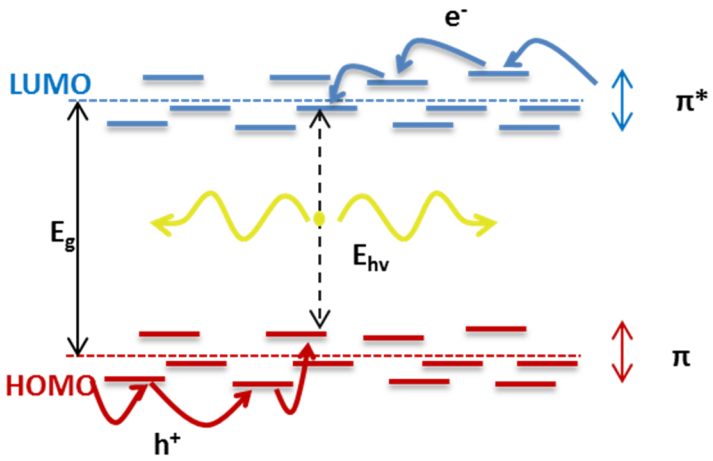


Figure 2-1 Schematic showing energy levels of a conjugated molecule π

2.2.2 Injection of charges

The injection of charge carriers at the electrode/organic, organic/organic interface is vital for OLED device performance. It decides the majority and the minority current which is a critical factor for the recombination rate and efficiency.

2.2.2.1 Metal/organic semiconductor interface

For metal/organic interface, the Mott-Shockley model (MS) which has been validated in the metal/inorganic semiconductor used for the early studies. The M-S model relies on two assumptions: (i) the vacuum levels are aligned at the interface; (ii) the energy bands are bent in the space charge layer to align the bulk Fermi level E_F [76]. Figure 2-2 shows the empirical M-S model of the metal /semiconductor interface. In the thermal equilibrium state, the Fermi level is constant across the whole system. The work function difference between the electrode and the semiconductor (also voltage across the space charge layer) is the built-in potential, V_{bi} ($eV_{bi} = |\Phi_m - \Phi_{org}|$). The barrier for hole injection,

Φ_p is defined as $I - \Phi_m$, where I is the ionization energy. The electron injection barrier corresponds to $\Phi_m - \chi$, where χ is the electron affinity.

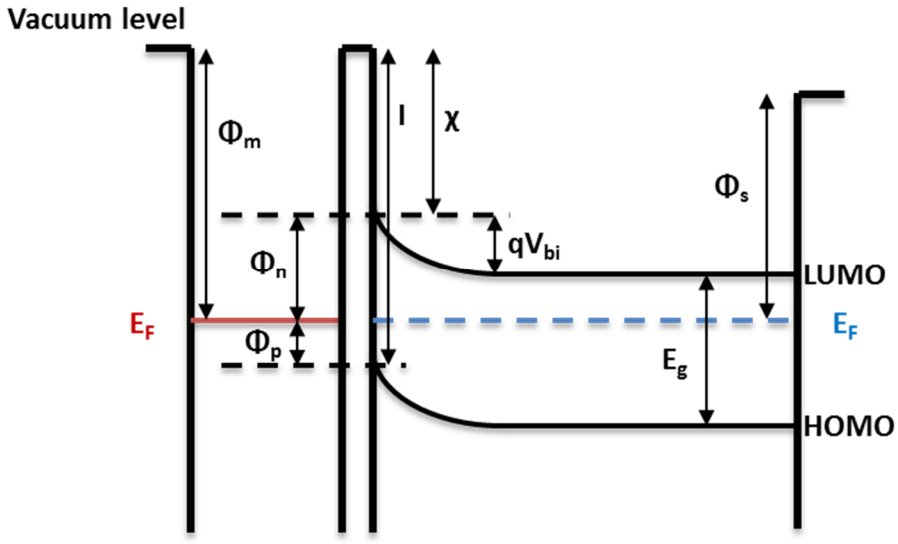


Figure 2-2 Energy diagram of Mott-Schottky model at the metal/inorganic semiconductor interface

However, recent studies [76] revealed that the vacuum level alignment is not valid in most of the metal/organic interfaces. The vacuum level is shifted with respect to the interfacial dipole formed at the interface. Figure 2-3 shows the energy model of the metal/organic interface with an interfacial dipole. There is an offset Δ of the vacuum level difference between metal and the organic semiconductor. The built-in potential is adapted to be $eV_{bi} = |\Phi_m + \Delta - \Phi_{org}|$. The formation of the interfacial dipole is not fully understood. There are several speculative explanation for it: charge transfer, mirror force, surface rearrangement, chemical interaction, interfacial state, permanent dipole and Pauli's repulsion [76]. Besides, for the assumption of Fermi level alignment, Ishii et al. have shown that there are some cases that cannot reach thermal equilibrium in the metal /organic interface [76]. The Fermi level alignment is formed under the condition that there are enough charge carriers (impurities) in the organic semiconductor.

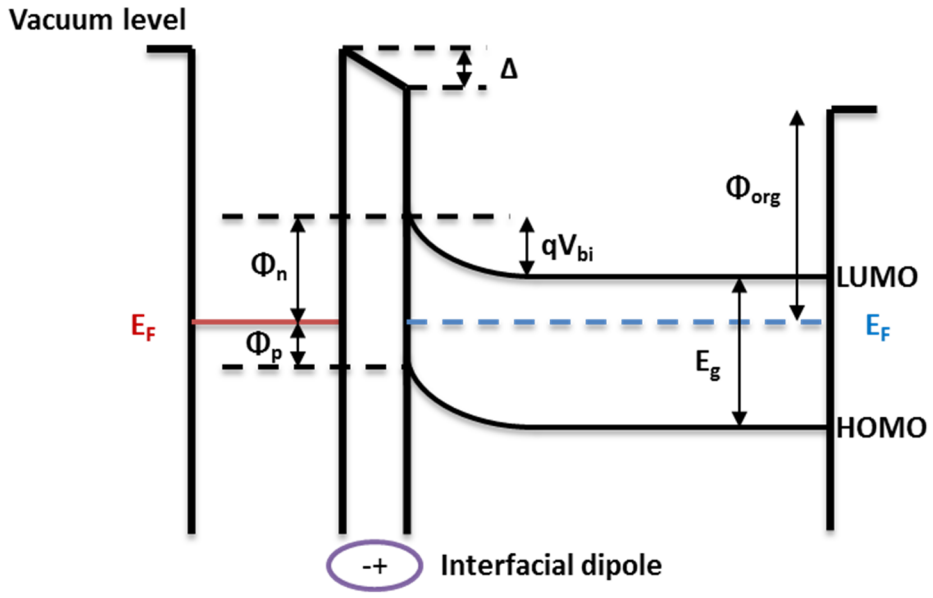


Figure 2-3 Energy diagram of the metal/organic interface with band bending and an interfacial dipole

Apart from the MS model, the Richardson-Schottky (RS) model is also studied for the metal/organic semiconductor interface. In 1901, Richardson published the thermionic emission law [77]. It described the thermal assisted electron emission of a metal surface in a vacuum. This classic model is applied for electron injection from metal to crystalline semiconductor. Figure 2-4 (a) illustrates the RS thermal emission in a metal/semiconductor interface. The electron emission current is found to increase with the square of temperature and decrease exponentially with the work function difference (between metal and crystalline semiconductor).

$$J = A_G T^2 \exp\frac{-W}{k_B T},$$

$$W = \Phi_m - \chi, \qquad \textbf{Equation 2-1}$$

$$A_G = \lambda_R A_0 = \frac{\lambda_R 4\pi m^* k_B^2 e}{h^3}$$

where T is the temperature, k_B is the Boltzmann constant, W is the work function difference between metal (Φ_m) and electron affinity of the crystalline semiconductor (χ), A_G is the Richardson's constant, λ_R is the material correction constant, m^* is the effective mass of an electron, e is the charge of an electron, h is the plank's constant, A_0 is the universal Richardson's, approximately 1.20173×10^6 $Am^{-2}K^{-2}$.

An improved model with consideration of the Schottky effect is provided by Bethe [78]. The injection current is modified to be,

$$J_{RS} = \frac{4\pi m^* e}{h}(k_B T)^2 \exp\left(\frac{-W}{k_B T}\right) \exp(f)^{\frac{1}{2}} \left[\exp\left(\frac{eV}{k_B T}\right) - 1\right],$$

$$f = \frac{e^3 E}{4\pi\epsilon\epsilon_0 k_B^2 T^2}$$

Equation 2-2

Where W is defined as the energy difference of metal work function and electron affinity of the semiconductor, similar to Equation 2-1, E is the electric field at the interface, V is the applied voltage. The second exponential term $\exp(f)^{\frac{1}{2}}$, which is related to the Schottky effect, manifests that the electric field lowers the barrier height induced by the image force. The third exponential term $\left[\exp\left(\frac{eV}{k_B T}\right) - 1\right]$ describes the effect of the applied voltage with doping in the semiconductor. It further decreases the barrier height. The -1 is used for current balance, so the injection current vanishes without applied voltage.

However, the model is not suitable for amorphous organic semiconductors, as the electronic states are highly localized, charge carrier transport by hopping, not a ballistic motion for energetic disorder[79].

Another model is the Fowler-Nordheim (FN) law applied for the tunnelling effect [80]. The model is built in the presence of a high electric field where an electron from a metal with lower Fermi level tunnel through the triangular barrier to a semiconductor. Figure 2-4 (b) shows the FN tunnelling behaviour. The tunnelling current is given as:

$$J_{FN} = \frac{e^3}{8\pi hW} E^2 \exp\left[-\frac{8\pi\sqrt{2m^*}W^{3/2}}{3heE}\right]$$

Equation 2-3

Where E is the electric field at the interface, m^* is the effective mass of charge carrier, W is the barrier height in work function where for electrons is $W = \Phi_m - \chi$, for holes is $W = I - \Phi_m$, where χ is the electron affinity of the semiconductor and I is the ionization energy of the semiconductor.

In order to consider these multiple charge injection mechanism in the organic material, Davids et al. [81] present a unified model which includes the thermal emission, tunnelling, and the interfacial recombination current. Figure 2-4 (c) shows a diagram of the unified metal/semiconductor interface model. A hole injection current is described as,

$$J_{hole} = -J_{RS} - J_{FN} + J_{Rec}$$

$$J_{Rec} = \frac{AT^2}{N} p(L)$$

Equation 2-4

Where A is the Richardson's constant, N is the density of states, and $p(L)$ is the hole concentration in L (length of the device).

The electron injection J_{RS} and J_{FN} is represented as a negative current. Moreover, the recombination current is a reversed process for thermal emission and tunnelling. The interfacial recombination current is proportional to the density of holes at the interface.

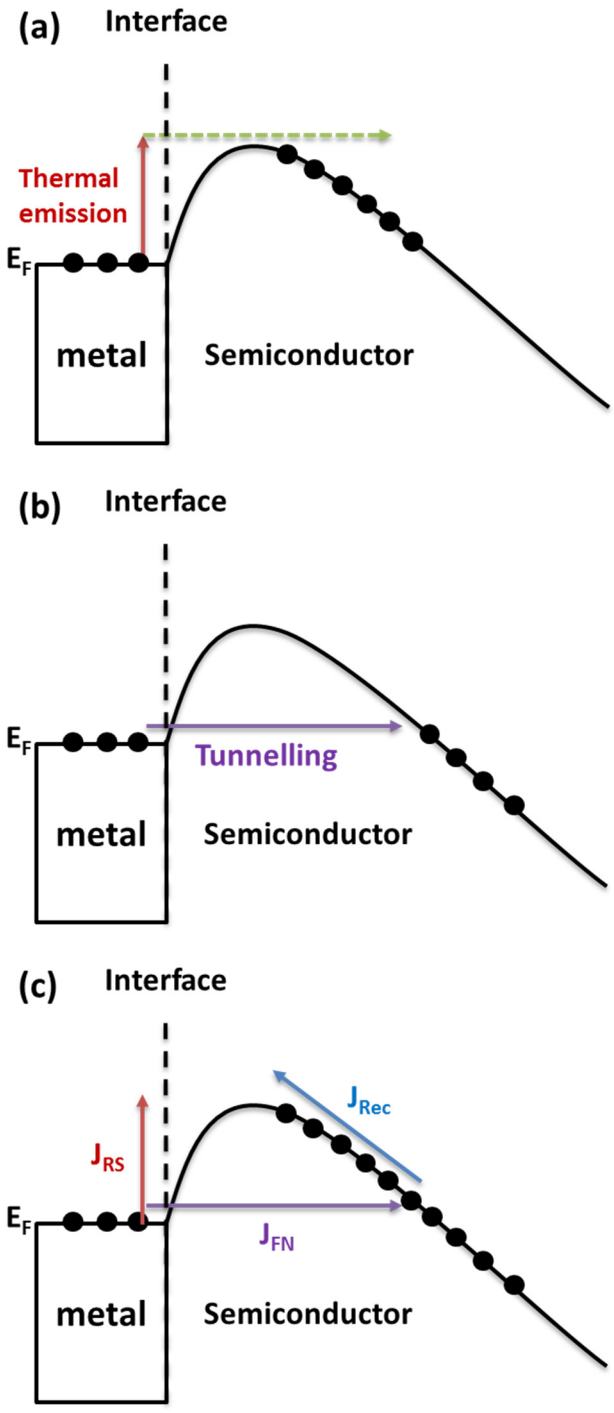


Figure 2-4 Illustration of charge injection from metal to semiconductor through (a) Richardson-Schottky thermal emission (b) Fowler-Nordheim tunnelling and (c) Unified model of thermal emission, tunnelling and interfacial recombination effects

The RS thermal emission and FN tunnelling are classic models for charge injection at the metal/ crystalline semiconductor. These processes are also verified in experiments that can be applied to organic semiconductors under certain circumstances. For example, the Arrhenius temperature dependent current density ($\ln J \propto T^{-1}$) [82], the Poole-Frenkel field dependent current density ($\ln J \propto \sqrt{E}$) [71], the FN tunneling current ($\ln J/E^2 \propto E^{-1}$) [83] have been reported on OLED device characteristics in literatures before. These processes imply that there is a strong electronic coupling between the lattice structures which forms the valence and conduction bands. This leads to a long scattering length compared to the interatomic separation. However, in an organic semiconductor, the molecules are bonded by the van der Waals [84-87] bonds which is a weak coupling. Thus, an injection current would be weaker than expected based on energy barriers and the Arrhenius scale becomes sublinear [88]. Bassler et al. [89, 90] have developed a model that consider (i) the image charge at the electrode, (ii) charge transport hopping, (iii) energy disordered in the organic semiconductor. Since then, there are studies that investigate the charge injection models based on a Gaussian density of states (DOS) distribution in organic semiconductors [91-94]. More recently, Coehoorn et al. [95, 96] investigated a three-dimensional charge carrier injection model. And the energy disorder are categorized into spatially uncorrelated energetic disorder described by extended Gaussian disorder model (EGDM) and spatially correlated disorder described by extended correlated disorder model (ECDM). The modelling of the interface of a metal and organic semiconductor has iterated from injection current equations to statistical models based on the Gaussian disorder nature of organics. The current density models are more accurate, but the price is the complexity and computation power for the development and application of the models.

Figure 2-5 shows a one-dimensional charge-injection hopping model at the metal and the organic semiconductor interface.

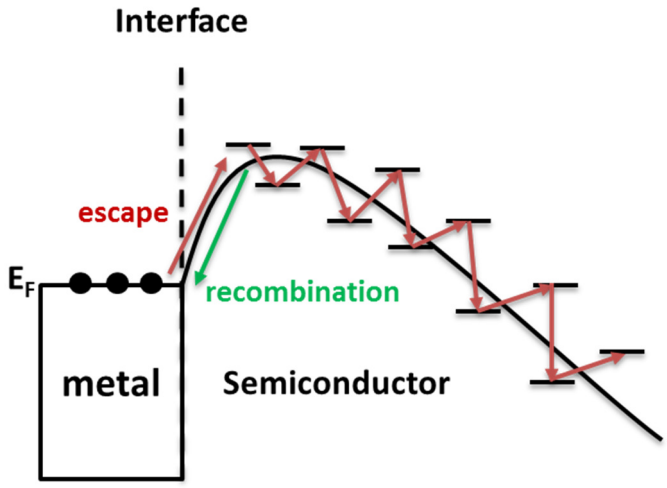


Figure 2-5 Charge injection by hopping at the interface of a metal and a disordered organic semiconductor

2.2.3 Charge transport in organic layers

For charge transport inside the organic layers, there are two main types of physical mechanisms that have been applied to represent the conduction: (i) hopping, the charges "hop" between localized energy states; (ii) trapping, charges transport through extended delocalized energy states, which is interrupted by traps.

2.2.3.1 Space charge limited current

The space charge concept is used to describe bulk-controlled conduction in the organic layer where both types of charge carriers inject into the bulk of organic layer and form a space charge layer. It modifies the electric field and strongly influences the current density.

The classical SCLC model was first follows the equation developed by Mott and Gurney in 1940 for a trap-free semiconductor sandwiched between electrodes [97].The inter-electrodes are separated by a distance L which is assumed to be greater than the transverse dimension to minimize the effect of the thermal carrier. The current follows a set of equations,

$$J = -\rho\upsilon$$

$$\frac{dE}{dx} = \frac{\rho}{\epsilon} \qquad \textbf{Equation 2-5}$$

$$E = -\frac{dV}{dx}$$

where ρ is the space charge density, υ is the charge drift velocity, $E$is the electric field, ϵ is the electrical permittivity of the material and V is the electric potential. The velocity increases monotonically with the electric field, and the current density becomes,

$$\upsilon = -\mu E \qquad \textbf{Equation 2-6}$$

$$J = \rho\mu E$$

By inserting Equation 2-5 to Equation 2-6, the current density becomes

$$J = \epsilon\mu E\frac{dE}{dx} \qquad \textbf{Equation 2-7}$$

Integrating Equation 2-7 for a steady state (stable) current,

$$\int_0^x J dx = \int_0^x \epsilon\mu E(x) dE(x) \qquad \textbf{Equation 2-8}$$

Where x is the thickness. If the boundary condition $E(x = 0) = 0$ is applied, we get

$$E(x) = \sqrt{\frac{2Jx}{\epsilon\mu}} \qquad \textbf{Equation 2-9}$$

By using Equation 2-5, the voltage difference is,

$$V(x) = \frac{2}{3}\sqrt{\frac{2J}{\epsilon\mu}} x^{3/2} \qquad \textbf{Equation 2-10}$$

By reshaping the equation, we obtained the Mott-Gurney equation,

$$J_{SCLC} = \frac{9}{8}\varepsilon\varepsilon_0\mu\frac{V^2}{d^3} \qquad \textbf{Equation 2-11}$$

where d is the device thickness.

The space charge limited current (SCLC) was first proposed for crystalline semiconductors by Lampert and Mark [98]. The SCLC would be valid under the assumption of [71]:

- The density of (at least one type of) injected charge carriers is higher than the thermal equilibrium, the injection limited boundary is neglected
- Only unipolar current is considered
- Free of intrinsic carriers and trap charges
- Diffusion current is negligible
- The charge carrier mobility is independent of electric field

To verify that the OLED current is limited by space charge, Mori et al. simplify the assumption to two conditions must be satisfied [99]:

- ✓ The charge is the same as the injection current from the ohmic contact

- ✓ The dielectric relaxation time[3] of the material is greater than the charge carrier drift time[4] between both electrodes

The SCLC conduction model is accepted for the description of low carrier mobility across the organic layers. However, Mori et al. [99] have shown in an experiment that both the conditions are hard to satisfy as

- × In multilayer OLEDs, the charge injection at the metal/organic can be ohmic. But it is not ohmic at the organic/organic junction.
- × In the presence of a strong electric field, the apparent dielectric time is shorter than the drift time in an experiment

If the constant mobility assumption is discarded, a field dependent mobility (without traps) can be resolved. Murgatroyd [100] gives an analytical Poole-Frenkel (PF) field dependent mobility,

$$\mu(E) = \mu_0 \exp\left(\beta\sqrt{E}\right) \qquad \textbf{Equation 2-12}$$

where μ_0 is the zero field mobility, β is the characteristic parameter of the dependence in an electric field.

The PF mobility has been reported in several amorphous molecule materials and polymer materials[101]. An analytical solution of trap-free SCLC that combines with the PF field dependent mobility [100] can then be developed in the form,

$$J_{SCLC}^{(PF)} = \frac{9}{8}\varepsilon\varepsilon_0\mu_0\frac{V^2}{d^3}\exp\left(0.89\beta\sqrt{V/d}\right) \qquad \textbf{Equation 2-13}$$

With the trapping effect ignored, the SCLC is actually the maximum physically-possible unipolar current in a sample at a given applied voltage. Only in the case of double-carrier injection that mutually compensates part of the space charge, the current can exceed the SCLC value.

[3] The relaxation time is defined as the time required for the material to restore neutrality, $\tau_r = \frac{\varepsilon\varepsilon_0}{\sigma}$, where σ is the apparent conductivity of the material

[4] The drift time is defined as the time required for a charge carrier (hole or electron) drift from one electrode to the other, $t_D = \frac{d}{\mu E_{av}}$

2.2.3.2 Trapped charge limited current

With traps existing in the organic samples, the current is generally smaller than the SCLC. The quadratic dependence is only valid when the traps are in discrete energy level or filled up. In order to consider the trapping effect, the SCLC **Error! Reference source not found.** can be modified to include a ratio $\theta = n/(n + n_t)$ of free carriers to the total number of carriers [100].

$$J_{SCLC} = \frac{9}{8}\varepsilon\varepsilon_0\mu\frac{V^2}{d^3}\theta$$

$$\theta = \frac{\rho_f}{\rho_f + \rho_t}$$

Equation 2-14

The ratio θ is dependent on the electric field. ρ_f and ρ_t are the free and trapped charge densities.

Due to the presence of traps, most of the injected holes are localized and not contribute to the current flow. The traps are gradually filled up with increasing electric field. The current increases faster than the quadratic field dependence until all the traps are filled. The voltage dependence current are determined by the density and energy distribution of the trapping state.

For organic semiconductors, the distribution models of the trap energy is similar to that of an insulator which the energy distribution is exponential [71, 100, 102, 103],

$$H_t(A) = \frac{\rho_t}{A_t}\exp\left(\frac{A - A_{LUMO}}{A_t}\right)$$

Equation 2-15

where A is the discrete energy level ($A \leq A_{LUMO}$), A_{LUMO} is the LUMO band energy, A_t is the characteristic energy of the distributions of traps, ρ_t is the total density of traps.

For the trap-charge limited current (TCLC) can be determined analytically with the exponential trap distribution [102, 104],

$$J_{TCLC} = \rho_C\mu e\left(\frac{\varepsilon\varepsilon_0 l}{N_t e(l+1)}\right)^l\left(\frac{2l+1}{l+1}\right)^{l+1}\frac{V^{l+1}}{d^{2l+1}}$$

$$l = A_t/k_BT$$

Equation 2-16

where ρ_C is the effective density of states in the LUMO band.

However, it is hard to get an analytical solution in an OLED device which includes the effect of background doping, the effect of Al Schottky contact and the effect of electric field on mobility. There are three different voltage dependence shown in SCLC/TCLC equations (Equation 2-11, Equation 2-13

and Equation 2-16), it could be quadratic ($J \propto V^2$), exponential ($J \propto \exp(\sqrt{V})$), power law ($J \propto V^l, l > 2$) or a mix of the three equations which is valid according to different voltage bias. Thus, the current-voltage characteristics are then described by numerical solutions. For example, Jain et al. [105] have shown a $J \propto V^3$ law fits better with a doped organic material with schottky contact.

2.2.4 Tandem structure OLED

In order to achieve high brightness, the tandem structure OLEDs (also known as stacked OLEDs), with multiple EL units connected in series, have been introduced. Charge generation layer is used to connect different EL units. For TOLEDs with N (N>1) EL units, N times emission is obtained. In contrast with conventional single EL layer OLEDs with similar current density, the luminance and driving voltage increases by N times. The tandem structure is popular for inorganic [106, 107] and organic [108-110] solar cells. The power conversion efficiency is improved by the stacking of multiple photoactive layers with different absorption spectra. The TOLED is gaining attention for its improved luminous efficiency and OLED lifetime [56, 111-113]. In conventional OLEDs, a high luminance often requires a high current density resulting in the degradation of organic material and a decreased lifetime. Therefore, the high current efficiency of TOLEDs avoids the aging effect at high current.

The idea of the tandem structure dates back to the stacked inorganic semiconductor laser developed by Kim et al. [114]. Kim demonstrates a semiconductor laser consisting of three p-i-n multi-quantum well active regions, a 233% differential efficiency[5] is measured.

The research of stacking multiple ELs for OLEDs started from the topic of full-color, tunable organic displays. Shen et al. [115] presented a three-color stacked OLED device in 1997. The OLED structure is shown in Figure 2-6 (a). Three OLEDs with red, green and blue are stacked vertically. Moreover, electrode layers are grown between each individual element in the stack OLED. Figure 2-6 (b) shows a top view of the stacked OLED with its electrode connections. The stacked OLED allows the tuning of OLED color by different emitting layers. Later, Gu et al. [116] also developed a similar structure stacked OLED with an insulating layer to allow independent driving of each OLED.

[5] The differential efficiency (also known as slope efficiency) of a laser is obtained from the slope of the optical power P_O versus current I. It is defined as $\eta_d = \frac{2e}{h\nu} \cdot \frac{dP_O}{dI}$, where e is the electron charge, $h\nu$ is the photon energy.

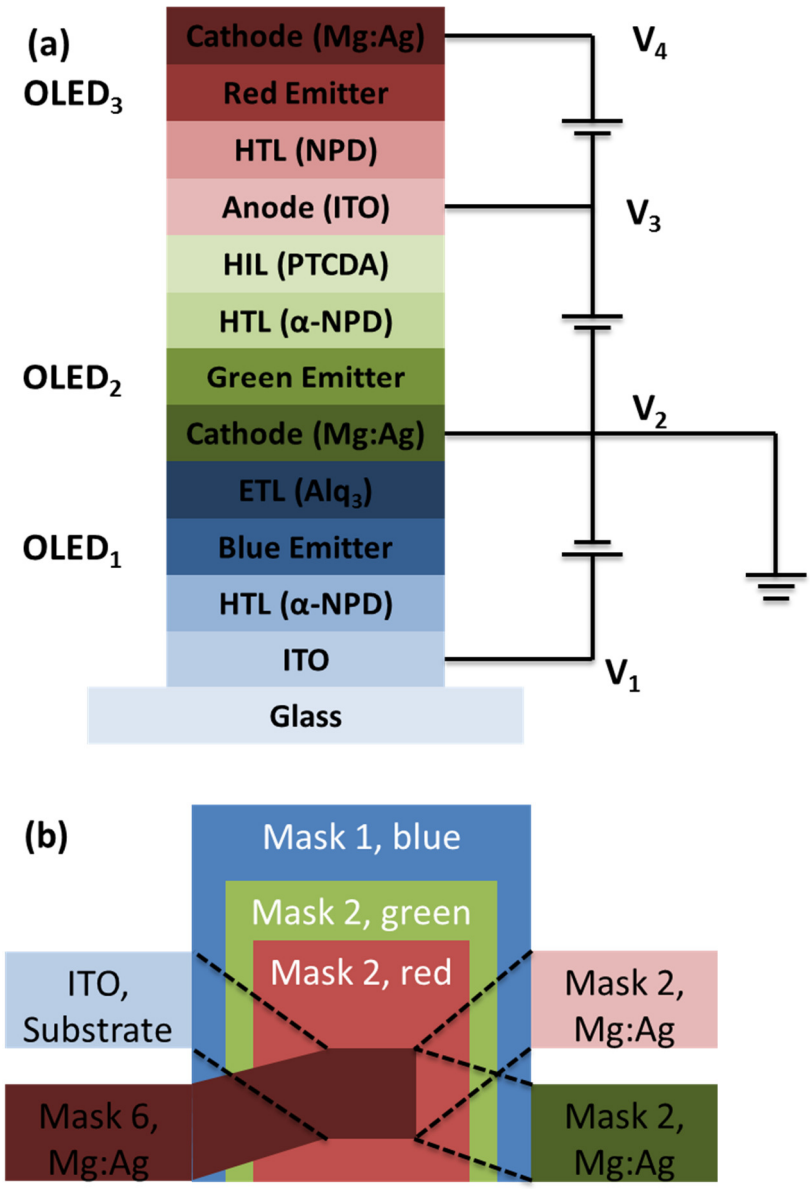


Figure 2-6 (a) schematic of the stacked OLED developed by Shen et al. (b) top view of the stacked OLED with electrode connections (source [115])

The approach of employing electrical connection between the stacked OLED elements is not practical. It requires power supplies for each OLED element. And the complexity of the OLED is not suitable for general display applications.

After that, in 2003, Kido et al. [55] developed the first tandem structure OLED (named as Multiphoton Emission, MPE, organic EL device) which employed charge generation layers (CGL) to connect the EL units. Conductive materials, ITO, V_2O_5 are employed for the CGL to injection holes and electrons. Only two electrode connections (anode and cathode) are required. A high quantum efficiency is achieved (approx. 48 cd/A) compared to a single EL unit OLED (approx. 17 cd/A) at the time.

The CGL material V_2O_5 is one type of the Transition Metal Oxides (TMO), which is believed to have exceptional properties for charge injection, extraction, and good transparency. Other TMO materials are also used as CGLs for tandem OLEDs, such as ReO_3 [117], MoO_3 [118, 119], WO_3 [120, 121]. In general, the main role of the TMO CGLs is to convert the electron current to a hole current. Figure 2-7 [120] shows an example of energy level diagram of TMO CGLs structure that consists BPhen:Cs_2CO_3 (EIL of EL1), WO_3 (CGL), and TCTA (HTL of EL2). The WO_3 possesses an n-type work function characteristics. The charge generations happen at the WO_3/TCTA heterojunction. The holes are injected to EL2. And the electrons are then injected to EL1 through tunneling at the BPhen:Cs_2CO_3/WO_3 interface.

On the other hand, several groups [117, 122, 123], including Liao and Tang [56] demonstrate tandem OLEDs that employed doped organic CGLs to form organic/organic PN junction. The organic/organic PN junction generates electron-hole pairs at the interface. Moreover, it is also important that good charge injection is achieved at the interface between the CGL structure and the EL units. Modifications of the EL units EIL and HIL are required to realize high power efficiency [124].

Terai et al. [125] verified the generation of holes and electrons through capacitance-voltage measurement. The capacitance of the CGL PN junction increases when forward bias applied, and extra charges are generated. Leem has [117] compared tandem OLEDs that employed TMOs and PN junctions as CGLs.

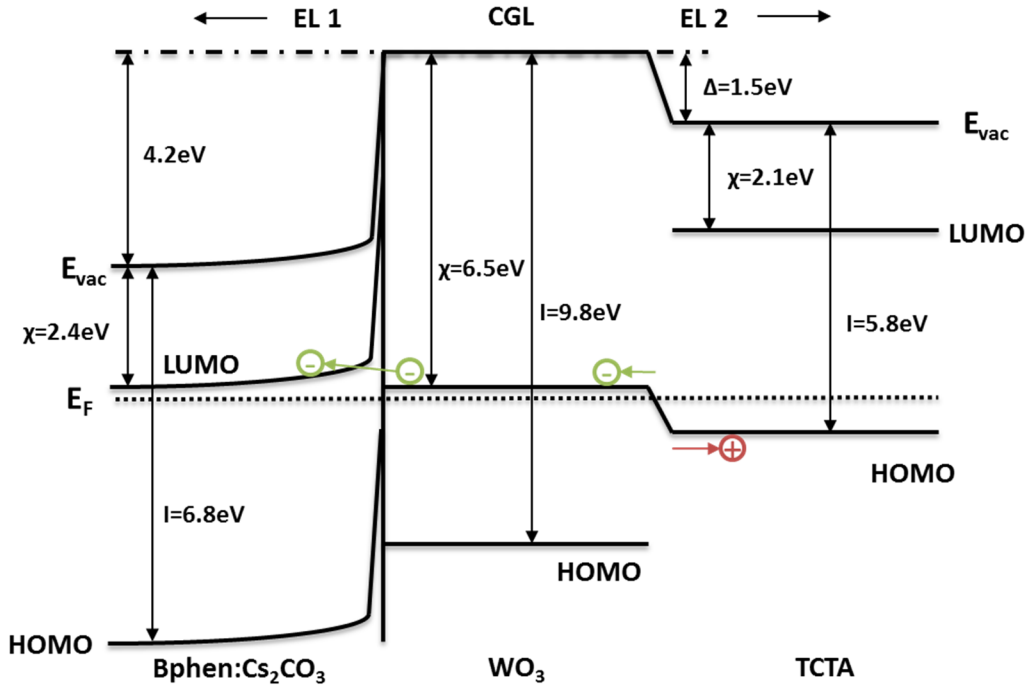


Figure 2-7 Energy diagram of the BPhen:Cs_2CO_3/WO_3/TCTA junction within a tandem OLED. X is electron affinity, I is ionization energy, and Δ is the interface dipole (source [120])

2.3 OLED SPICE model

As mentioned above, the OLED device can be modelled based on the energy bands, charge carrier hopping and trapping. We refer to these models as molecular models in this section. The molecular models are essential for the design of OLED devices. The process of developing OLED is complex, especially for multilayer OLED devices. And the vast majority of OLEDs have two or more layers. The molecular models are used to predict the characteristics of OLEDs before the OLED device is made. The model simulations are based on Technology Computer Aided Design (TCAD) tools, e.g. ATLAS from Silvaco®.

It is necessary to understand the electronic processes such as injection, charge transport, generation, and diffusion etc. But in the meanwhile these physics processes are complicated. It requires finite element simulations and/or Monte Carlo simulations [126]. In order to accurately simulate the response of an OLED device, 3-dimensional [96, 126, 127] molecular-scale simulations are usually applied, which reqiore a large amount of computational resources. On the other hand, for OLED microdisplay development, the OLED model is required to accurately describe the OLED characteristics as well as compatible to circuit simulators (e.g. Cadence). It is not realistic to apply the molecular models for CMOS driver circuit simulations. Therefore, we will explore the so-called compact models that use an equivalent circuit to represent the OLED characteristics.

The compact model is based on circuit simulator components in the standard SPICE (Simulation Program with Integrated Circuit Emphasis) library. Although the SPICE-based models are not showing the detail device physics as the previous mentioned molecular models, the simplified physical descriptions are represented by the SPICE components. Furthermore, the parameters of the SPICE components are extracted through measurement result. Relative high accuracy is achieved without the knowledge of the detail organic materials attributes, for example, hole/electron mobility, state density, and distribution, HOMO/LUMO energy levels.

2.3.1 Initial junction diode model for SPICE

The SPICE approach model can be dated back to 1970s the development of first silicon diode model for computer-aid analysis program. The program was named CANCER (Computer Analysis of Nonlinear Circuits, Excluding Radiation) [128] before it is renamed as SPICE [129, 130] later in 1972. The diode model is based on an inorganic junction diode. The diode model includes a bulk resister, a diode which based on a Schottky diode equation with an ideality factor, and two capacitors representing the diffusion and depletion layer charge storage. The effect of breakdown is not included. The large signal model is shown in Figure 2-8 (a). It is for DC analysis to determined the quiescent operating point of the circuit. Whereas the small signal model is used for transient and AC analysis.

The Schottky diode equation is,

$$I_D = I_S\left[\exp\frac{eV_D}{nk_bT} - 1\right] \quad \textbf{Equation 2-17}$$

where V_D is the diode voltage, n is the ideality factor, and typically varies from 1 to 2 for semiconductor material. If n is 1 for 'ideal' diode. I_S is the reverse saturation current. Figure 2-8 (c) shows the I-V plot of an ideal Schottky diode, I_S is the current for $V_D \leq 0$.

The charges on Q_1, Q_2 represent the diffusion and deletion layer charge storage effects. They are described as,

$$Q_1 = \tau_T I_D$$
$$Q_2 = C_0\int_0^{V_D}\frac{dV}{(1 - V/\phi)^{0.5}} \quad \textbf{Equation 2-18}$$

where τ_T is transit time, C_0 is the zero-bias junction capacitance, ϕ is the activation energy.

Moreover, for the small signal model, the diode can be seen as a resistor with conductance g_D, which is derived from Equation 2-17,

$$g_D = \frac{e}{nkT}\left(I_{D_0} + I_S\right) \quad \textbf{Equation 2-19}$$

where I_{D0} is the quiescent point current.

And the equivalent capacitance is the differential of Equation 2-19,

$$C_D = \tau_T g_D + \frac{C_0}{(1 - V/\phi)^{0.5}} \quad \textbf{Equation 2-20}$$

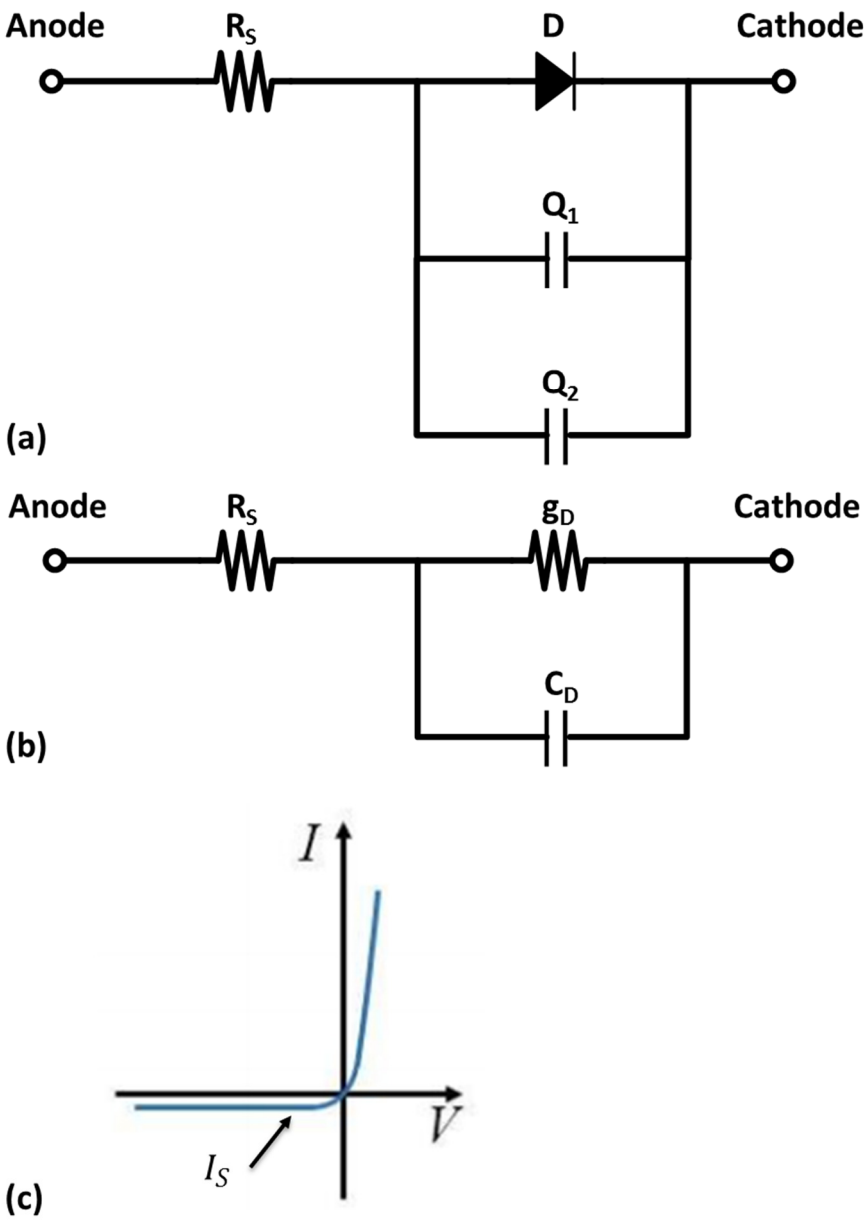


Figure 2-8 The model of the CANCER junction diode(a) large signal model (b) small signal model (source [128]) (c) Plot of the I-V characteristic according to the Schottky junction equation

2.3.2 Amorphous/crystalline heterojunction model

The conduction of organic semiconductor is similar to amorphous inorganic semiconductors. A SPICE model is developed by Marsal et al. [131] for amorphous/crystalline silicon heterojunctions (a-Si:H/c-Si). The model includes a diode, a space charge limited current resistor R_{SCLC}, and an ohmic resistor R_{ohmic}. The diode D describes the low voltage exponential current-voltage characteristics; The SCLC R_{SCLC} component describes the bulk-limited power-law increase which is controlled by the amorphous

silicon layer space charge. The ohmic resistor R_{ohmic} is parallel with R_{SCLC} which describes the resistance of amorphous silicon layer at low voltage bias. The R_{SCLC} is given by,

$$I_{SCLC} = KV_b^m \qquad \textbf{Equation 2-21}$$

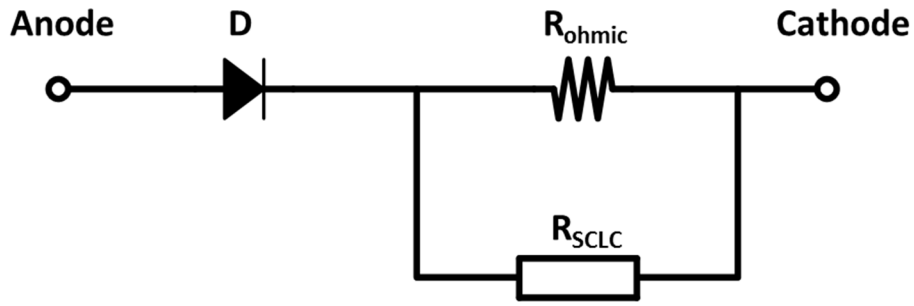


Figure 2-9 SPICE model for a-Si:H(n)/c-Si(p) heterojunction diode (source [131])

2.3.3 OLED SPICE model review

One of the very first studies of different OLED SPICE models and their ability to simulate the DC and AC characteristics was made by J. P. Bender et al. [132] in the 1990s. They employed a multilayer OLED, as shown in Figure 2-10 (a). An initial model was developed according to each individual layer, which is a so-called multi-diode SPICE model. The model is shown in Figure 2-10 (b). Each OLED layer is modelled as a capacitor shunted with a diode and a series resistor and a parallel leakage resistor. The capacitor describes the depletion layer capacitance which is extracted according to the thickness and the dielectric constant of the organic layer material. The resistors represent the low motilities of the organic layer materials. Another resistor is used to describe the sheet resistance of the ITO layer, a value of 30 Ω is extracted.

Moreover, a simplified single diode model is developed. As shown in Figure 2-10 (c), the model combines the components of different layers to a capacitor shunted by a resistor and a diode. The diode equation includes the ideality factor and the saturation current like Equation 2-17. The parameters are extracted through least-square curve-fitting. The ideality factor is extracted to be ~40, the bulk resistor is extracted to be 36 Ω, and the parallel capacitance is 2.65nF. The simplified model with a PN diode and a bulk resistor is able to fit the OLED electrical characteristics nicely.

Thus, the development of a SPICE model for each individual layer is not imperative. The SPICE model can be developed according to the dominant conduction mechanisms (e.g. charge injection, bulk limited) of the OLED. However, it is worth to mention that this model's capacitance is acquired by transient voltage-transient current measurement. And the DC and AC characteristics cannot be simultaneously modeled by the same set of model parameters.

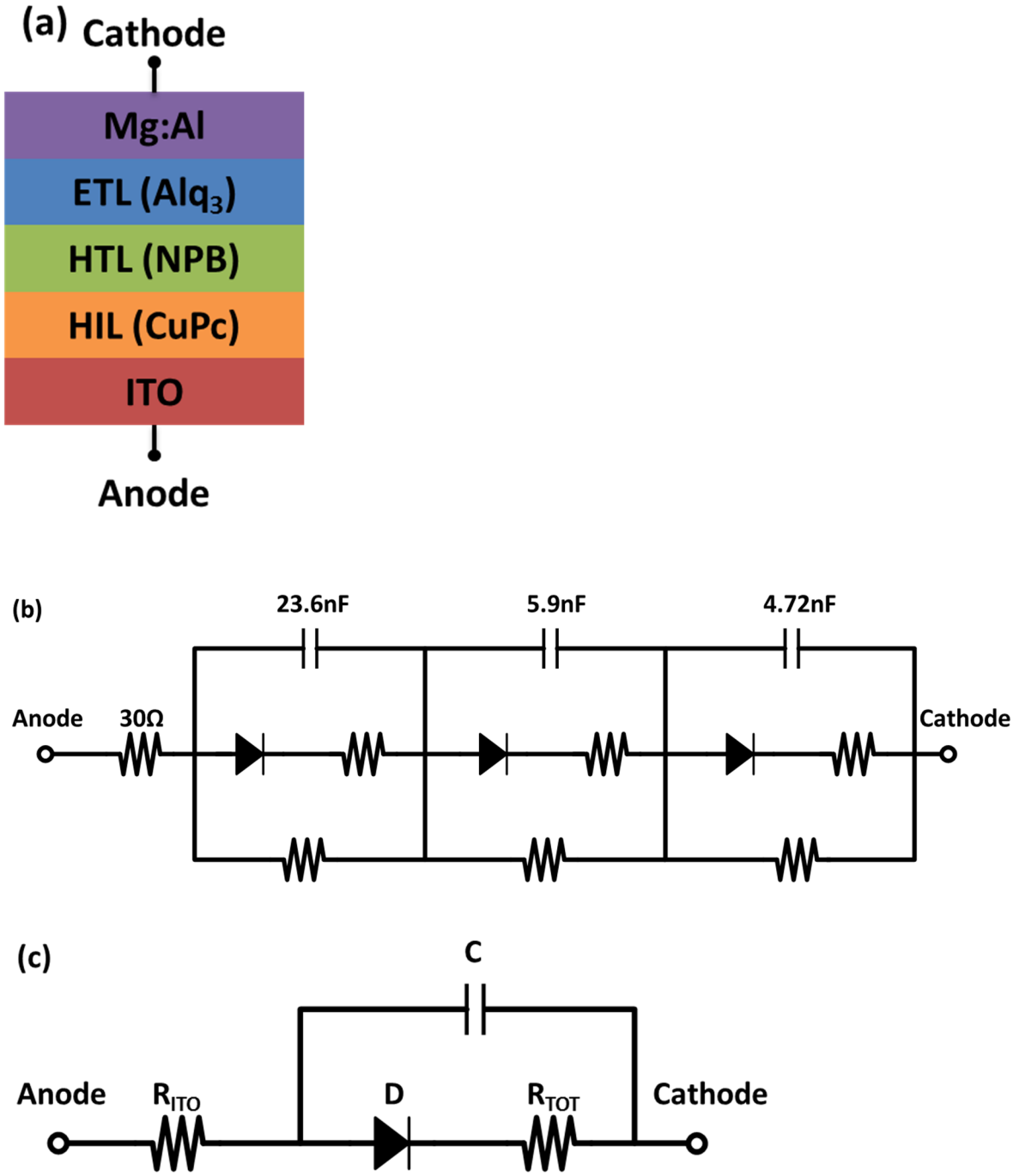


Figure 2-10 (a) OLED stack modelled (b) multi-diode SPICE mode (c) Single diode model (source [132])

Later, Jacobs et al. [133] applied a simple junction diode model for a monochrome small molecule OLED which include a diode, a series resistor, and a parallel capacitor, as shown in Figure 2-11. The diode component parameters are extracted through the DC I-V characteristic curve. The parallel capacitor C_{OLED} and R_{ITO} are calculated through the AC impedance spectra measurement. The R_{ITO} is approximately 15 Ω/□, and the COLED is about 200~400 pF/mm^2.

This is the first OLED model, which evaluates the OLED capacitance through impedance spectroscopy measurement. The extracted capacitance is not constant. It varies according to the bias voltage and frequency.

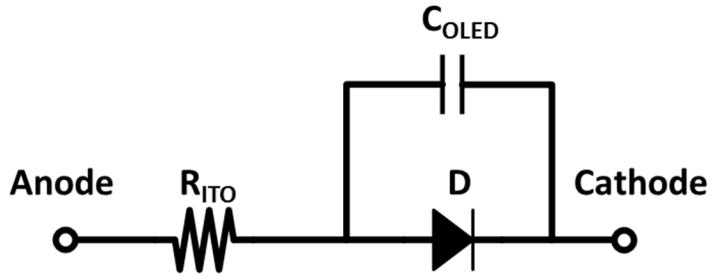


Figure 2-11 Equivalent circuit model

Li et al. [134] proposed a model which includes a voltage source, a diode, and a variable resistor, as shown in Figure 2-12. The voltage source V_{bi} correlates to the built-in voltage. The diode D is an ideal for reverse current rejection, without any resistance. The variable resistor R_S is used to describe the non-ideal ohmic contact (possibly including the SCLC effect).

However, the model does not include any capacitors for the AC and transient simulations.

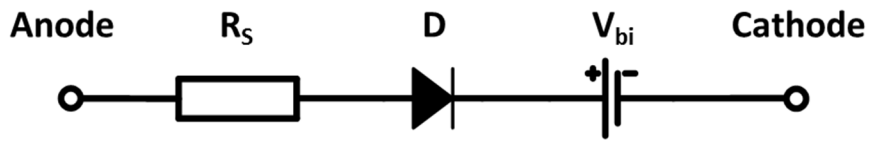


Figure 2-12 OLED model proposed by Li et al. (source [134])

Kanicki et al. [135] presented a model for Polymer OLEDs. As shown in Figure 2-13, the model includes three paralleled-connected diode-bulk resistors series, a parallel resistor R_P, and a parallel capacitor C_P. The diode and the series resistor pairs and R_P are obtained through the fitting of DC J-V characteristics. Each of the diode branches is dominant at a certain voltage region, where the effects of the other two branch are negligible. C_P is estimated by the dielectric constant of the polymer light-emitting layer. A good fit is achieved according to the paper. The approach is similar to a piece-wise curve fitting. However, it is not based on any physical mechanisms such as FN tunnelling, RS thermal emission, and space-charge-limited current, probably not suitable for other OLEDs.

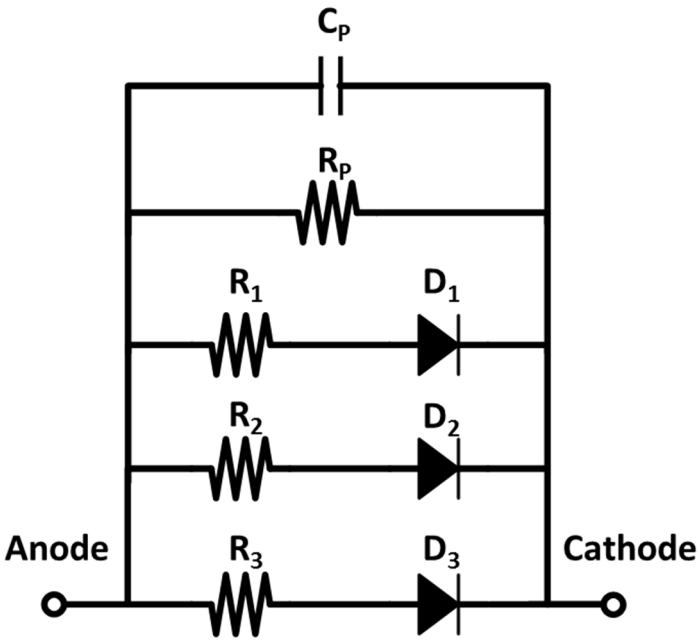


Figure 2-13 PLED SPICE model (source [135])

Buso et al. [72] presented the use of a model shown in Figure 2-14 to fit a multilayer OLED. The model includes a series resistor R_e which denoted the electrode ohmic resistance; a parallel resistor R_P representing the leakage resistance; a voltage source V_{bi} showing the OLED built-in voltage; an ideal diode D; and a variable resistor R_S, which is given by

$$I = A \cdot \exp\left(B \cdot V_{R_S}\right) \qquad \textbf{Equation 2-22}$$

The diode D is only for rejecting reverse current, not for a description of injection-limited current. The OLED static characteristic is fit by a relatively simple exponential function (Equation 2-22). However, the fitting is insufficient. Later, Lin et al. in the same group [136] present a model with piecewise-linear based resistor and capacitor to achieve an agreement between measurement and simulation data.

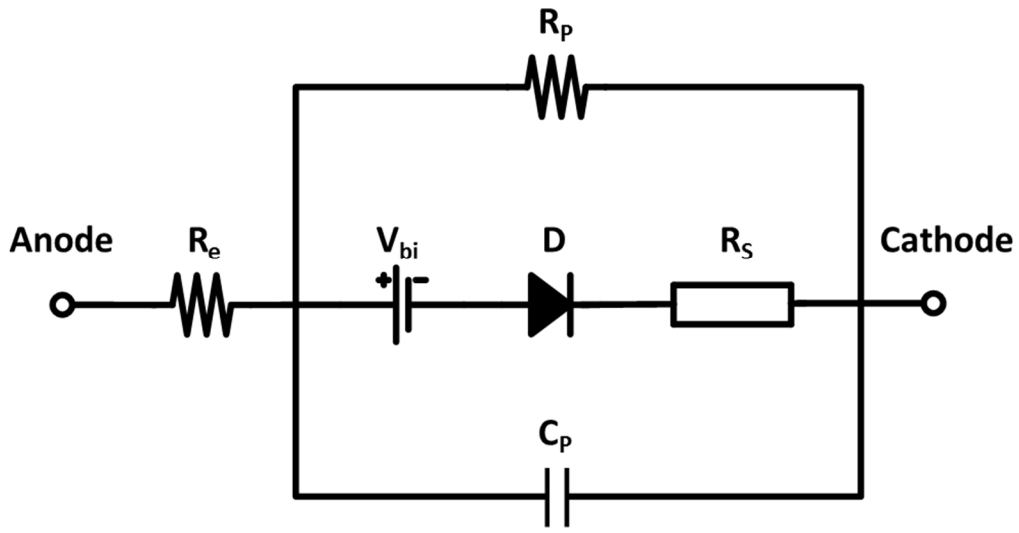


Figure 2-14 OLED equivalent circuit model used by Buso et al. (source [72])

Later, V. C. Bender et al. [74] proposed an OLED SPICE model for improving performance on capacitance-voltage (C-V) fitting. The SPICE model is shown in Figure 2-15 (a). The model has an electrode resistor R_e, a parallel resistor R_P, a parallel capacitor C_g and two diode branches. The first branch is formed by an ideal diode D_1, a built-in resistor R_{bi} and a built-in voltage V_{bi}, and a diffusion capacitor C_d in parallel with R_S. The second branch includes a series resistor R_S, an ideal diode D_2, and a voltage source V_O. This approach is close to a piecewise-linear method proposed by Lin [136]. As shown in Figure 2-15 (b), in region 1, both diode branches are off, the leakage current is represented by R_e+R_p. At region 2, the bias voltage is greater than V_{bi}, the simulated impedance is reduced to R_e+R_{bi} and a depletion capacitor C_d in parallel. In region 3, the applied voltage increases to higher than V_O, the impedance becomes R_e+R_{bi}//R_S[6]. The diode D_3 provides an extra path for discharge of the capacitor C_d.

The model takes advantage of the ideal diode to realise a piecewise linear model with SPICE components. However, the use of resistors cannot model the nonlinear OLED I-V characteristics. As shown in the paper, the model simulation deviates from the OLED I-V curve at some voltage range.

[6] // means resistors in parallel

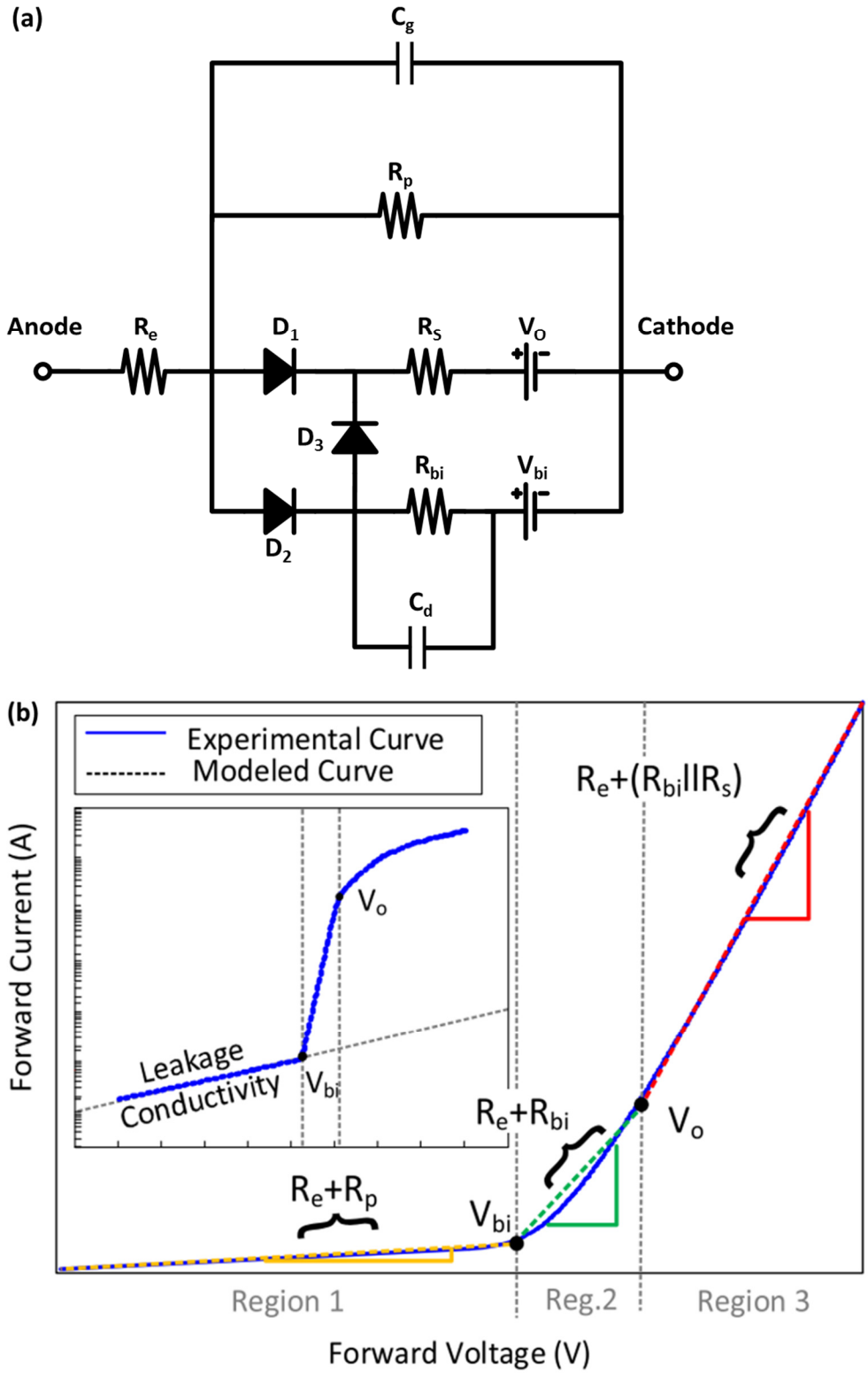


Figure 2-15 (a) OLED SPICE model proposed by V. C. Bender (b)simulated and measured I-V characteristics (source [74])

2.4 Characterization method

2.4.1 Measurement test bench

The test bench is shown in Figure 2-16. The OLED samples are probed using an Everbeing Multi probe station[7]. The DC steady-state, AC capacitance-voltage measurements are taken using a Keithley 4200-SCS Parameter Analyzer[8]. The DC current-voltage sweep measurement is performed through Kelvin (4-terminal) sensing method. Separate probes are used for current sourcing and voltage measurement. The impedance of the lead and the electrode contacts are eliminated. It is more precise than 2-terminal measurement for low impedance measurements.

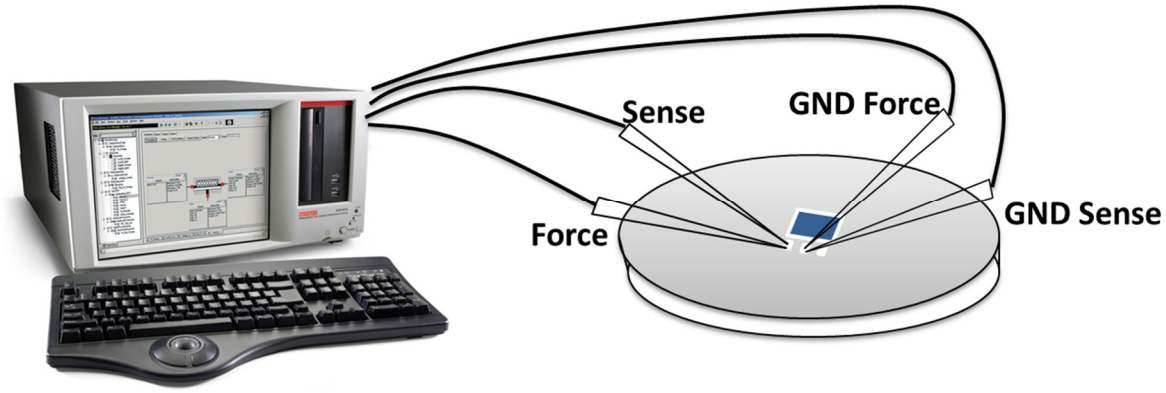


Figure 2-16 Block diagram of the measurement bench

2.4.2 OLED test samples

Both the conventional and tandem structure OLEDs are supplied by MicroOLED through the POLIS project. The OLEDs are deposited on silicon wafers as top-emitting structure to emulate the case of an OLED-on-CMOS microdisplay. Measurements have been taken on both pixelated (display matrix but without CMOS circuit beneath) and diode structure (no pixilation of OLED on substrate). Figure 2-17 shows the image of the tandem structure OLED samples. The diode structure samples have an active area of 0.44 cm^2. The active area of pixelated structure OLED is half, 0.22 cm^2. However, there is leakage at the edge of the pixelated structure when a voltage is applied between the cathode and anode electrode. The current-voltage curve is skewed by the edge effect Therefore, the modelling and calculation of the current density are measured by the diode structure OLEDs.

[7] http://www.probestation.tw/category-Probe-Station-pro-A.html
[8] https://uk.tek.com/keithley-4200a-scs-parameter-analyzer

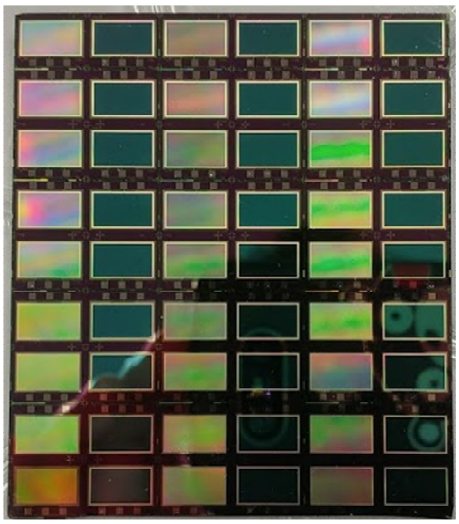


Figure 2-17 Image of OLED sample

2.4.3 Measurement error

The measurement accuracy depends on the sensitivity of the characterization instrument. It is challenging to measure the OLED at a low voltage bias, when current < 1 nA, impedance > 1 GΩ. The electrostatic voltage source from the connecting cables, test fixtures, and probes generate a noise current at the same scale as the measured current. Probe station shielding and guarded Triax cables are employed to reduce the electrostatic interference and leakage. A preamp control (PA CNTRL) terminal is used to provide precise small current scale measurement.

Table 2-1 shows the current and voltage source/measurement range and resolution of the Keithley 4200 SCS PA CNTRL. Both current and voltage sweep are performed to ensure the repeatability. Figure 2-18 shows an example current density-voltage (J-V) curve of the DC sweep measurement. The dual sweep[9] measurement indicates the OLED hysteresis effect. Both curves are similar except for low bias (< 4V), where the current source measurement is quieter than the voltage source's. The reason is that the voltage source measurement is susceptible to the electrostatic noise and leakage current, whereas the current source measurement avoids through the 4-wire configuration. Therefore, at low voltage, the DC J-V measurements are taken via current source measurement And both voltage source and current source are employed for high voltage measurement, depends on the requirement of the measurement points.

[9] Dual sweep: the source/measurement unit (SMU) sweep from start value to stop value, and then continue to sweep from stop back to start. Whereas for single sweep, the SMU only sweep from start to stop.

Table 2-1 Keithley 4200 SCS PA CNTRL current and voltage source and measurement characteristics

Voltage source/measurement range	Voltage measurement resolution	Voltage source resolution
210 mV	1 μV	5 μV
2.1 V	10 μV	50 μV
21 V	100 μV	500 μV

Current source/measurement range	Current measurement resolution	Current source resolution
1.05 pA	10 aA	50 aA
10.5 pA	100 aA	500 aA
100.5 pA	1 fA	5 fA
1.05 nA	10 fA	50 fA
10.5 nA	100 fA	500 fA
105 nA	1 pA	5 pA
1.05 μA	10 pA	50 pA
10.5 μA	100 pA	500 pA
105 μA	1 nA	5 nA
1.05 mA	10 nA	50 nA
10.5 mA	100 nA	500 nA
105 mA	1 μA	5 μA

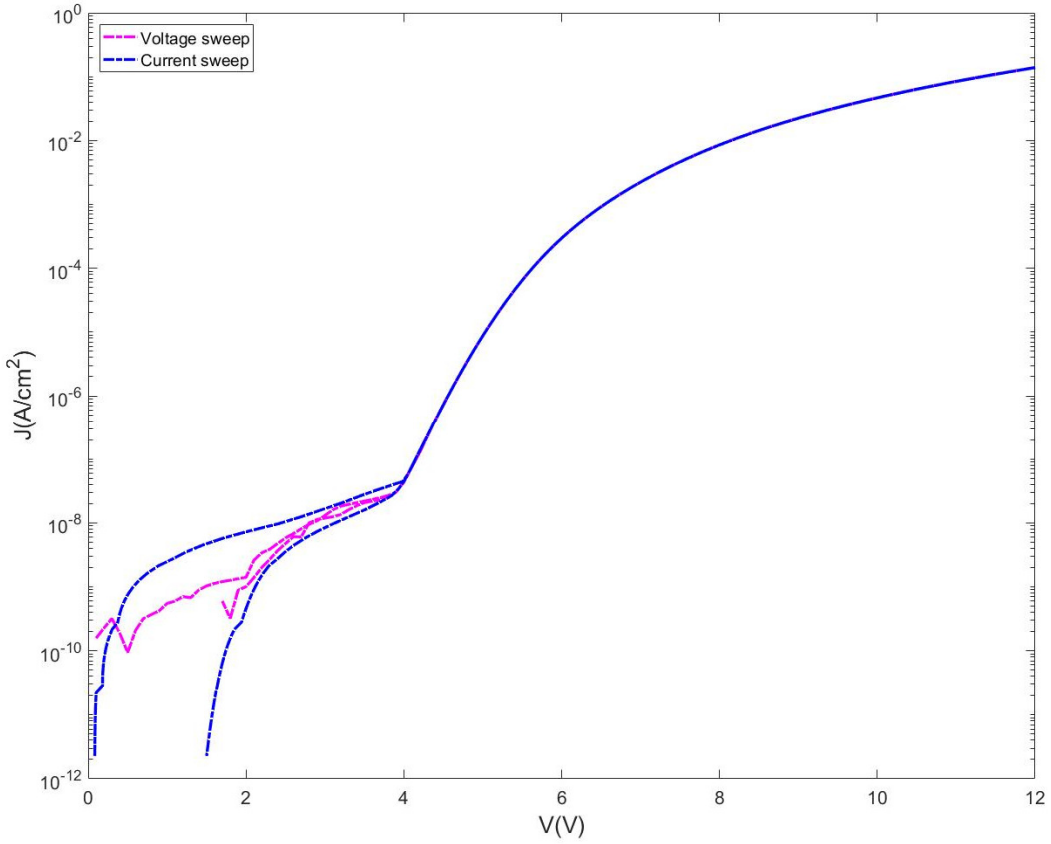


Figure 2-18 DC dual sweep measurement with voltage source (pink) and current source (blue), 30 second hold time, 1-second sweep delay

2.4.4 Low voltage hysteresis

As shown in Figure 2-19, below the threshold voltage at about 4V, a large hysteresis of the J-V curve is visible between an up sweep measurement and a down sweep measurement. The hysteresis effect gradually reduces with a longer sweep delay between each step. To achieve a negligible level of hysteresis, more than a 240 second delay is required. The recharging of deep traps [137, 138] is the cause of this transient J-V characteristic. For up sweep, with each step of voltage increase, the measured current overshoots initially to compensate the deep trap recharging current, and settles after a delay time. On the other hand, for down sweep, the deep traps release charges to generate a negative current. The zero current occurs at a positive bias.

A 10-second sweep delay is applied to remove most of the hysteresis in the steady-state J-V characteristics. Moreover, in the OLED SPICE model, this hysteresis behaviour is analytically represented by the layer capacitance.

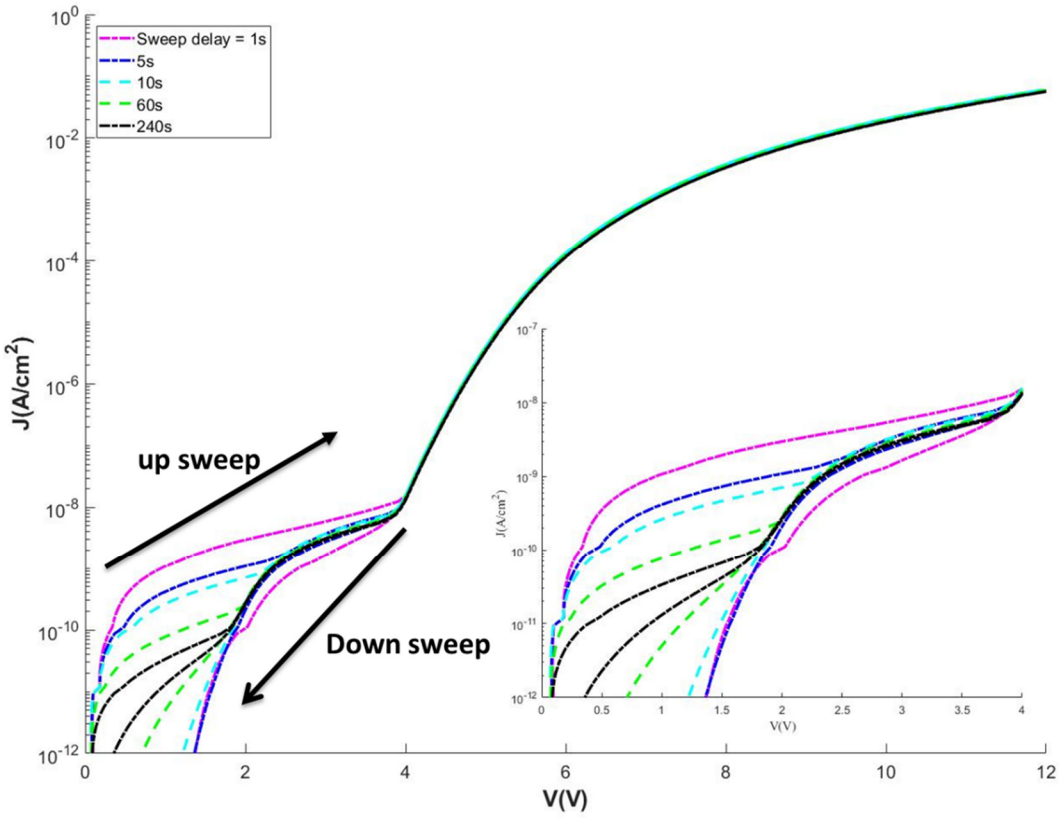


Figure 2-19 DC dual sweep measurements showing the subthreshold hysteresis effect by different sweep delay (1s, 5s, 10s, 60s, 240s); the inset shows magnification at 0 to 4V.

2.4.5 OLED sample variation

Manufacturing variation is a key technology challenge for OLED display panels. Both the display backplane and the OLED device are the key attributes to the variations. In this chapter, only the variation of OLED device is discussed. It is inevitable that there are variations between different OLED samples on the same wafer and on different wafers. It can be induced by the OLED patterning processes. The more complex the OLED structure is, the more difficult the quality control of OLED uniformity. Figure 2-20 shows the measurement of multiple OLED samples on the wafer shown in Figure 2-17. It is measured through voltage sweep (4 to 12V) and current sweep (<4V) with a 10 second sweep delay. In total 27 OLED devices are measured on the wafer. At high voltage, there are hardly any difference in the J-V curve. However, at low voltage, one of them is obviously an outliner (sample 26). Moreover, there are evident variations at the low voltage region for other OLED samples. The average and standard deviation of these J-V curves are shown in the Figure 2-20 inset. The standard deviation denotes the level of the variation. The variation is relatively high compared to the mean value at 2 to 4V.

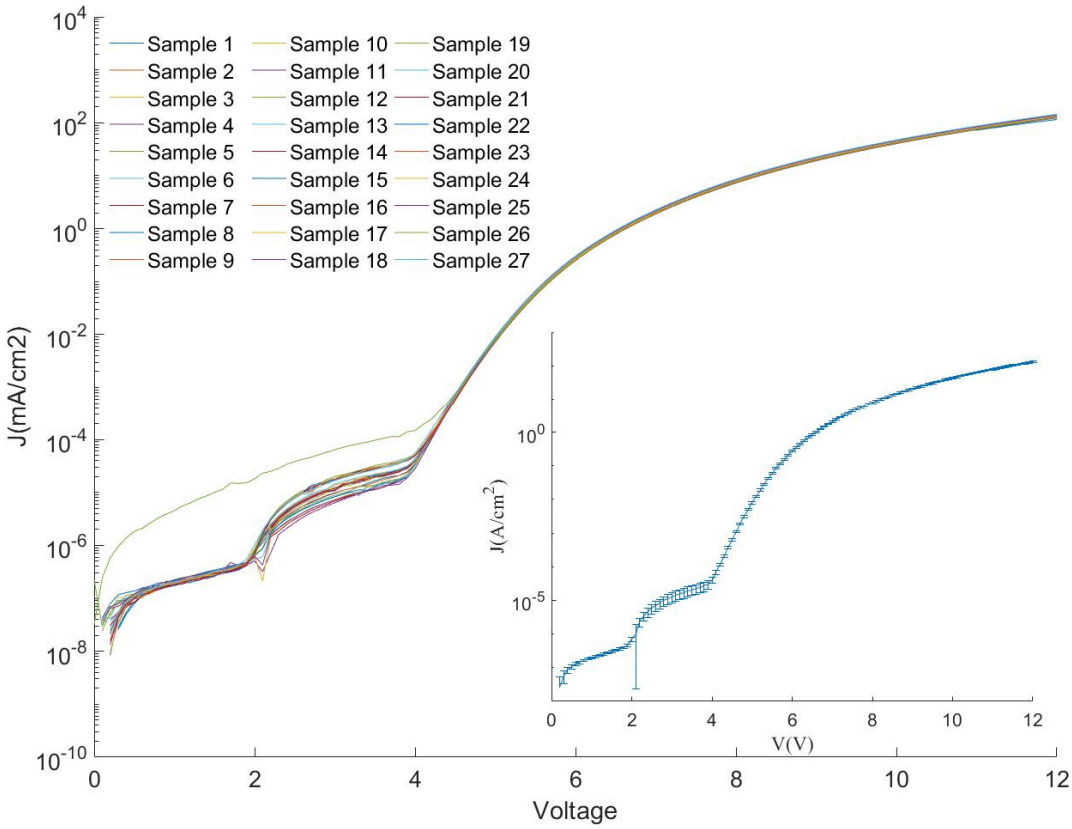


Figure 2-20 Voltage sweep measurement of multiple TOLED samples; the inset shows the mean J-V plot, and the error bar shows the standard deviation ±σ of the plot. (Outliner is ignored)

2.5 The conventional and tandem structure OLED

Figure 2-21 shows the schematic cross-section of the conventional single layer OLED (a) and the TOLED (b) that used for modelling in this section. Both OLEDs have blue, green and red emitting layers to achieve a white spectrum. There are two EL units in the TOLED. One is the deep-blue fluorescent emitter. The other composed of phosphorescent green and red emitters. A high-quality Charge Generation Layer (CGL) is deposited in between the EL units.

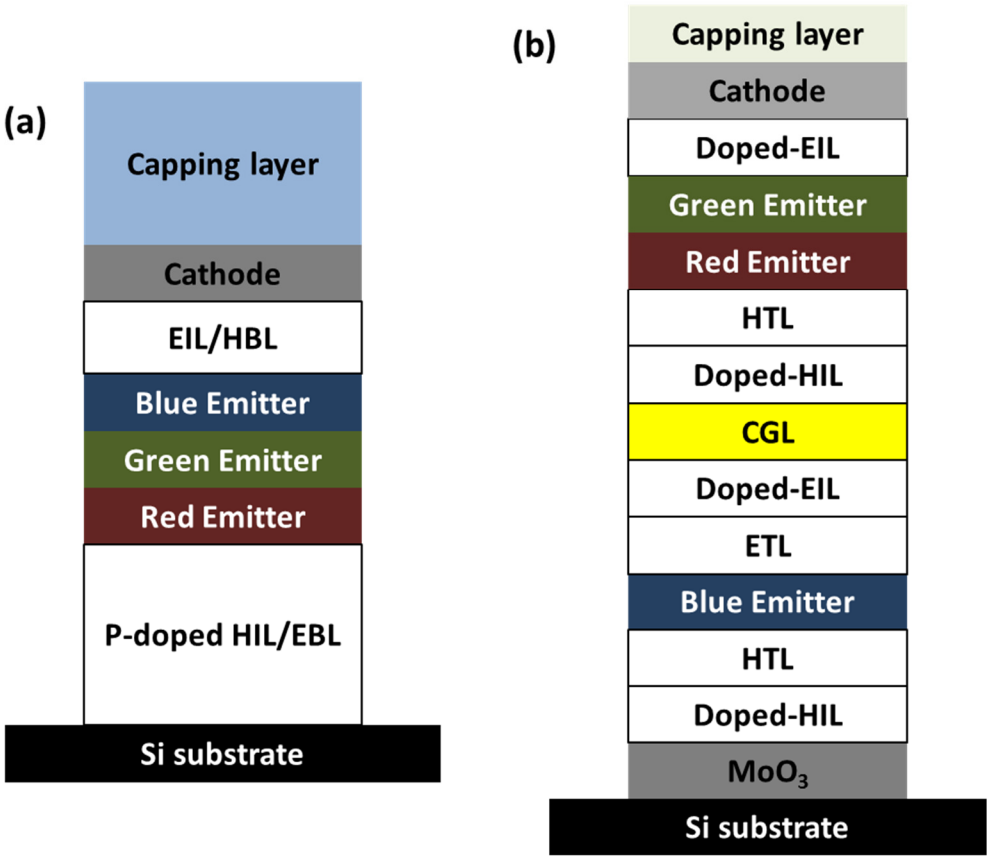


Figure 2-21 (a) Conventional single layer white OLED stack (b) white TOLED stack (thickness and material is not shown)

2.6 Single unit OLED SPICE model

The tandem structure OLED is comparable to two single unit OLED connected in series. It is worth to explore single unit OLED models regardless of some fundamental differences between them.

Figure 2-22 displays the J-V characteristics of the single unit OLED. For the applied voltage less than the threshold voltage (around 2V), the curve shows a linear leakage current. From 2V to 3V, the J-V curve starts an exponential increase similar to the injection-limited current like the RS Equation 2-2. Then, the slope curve starts to saturate at about 3V. Similar to the space charge limited current (**Error! Reference source not found.**), the J-V curve slope is close to a square rule in this region.

A typical SPICE model [72, 75, 139] was employed to model the single unit OLED, as shown in Figure 2-23. an In the electrical model, R_p is the leakage resistance, representing the low voltage diffusion current, V_{bi} represents the built-in voltage of the diode, D is a diode representing the charge injection component, R_{bulk} is the bulk-limited component.

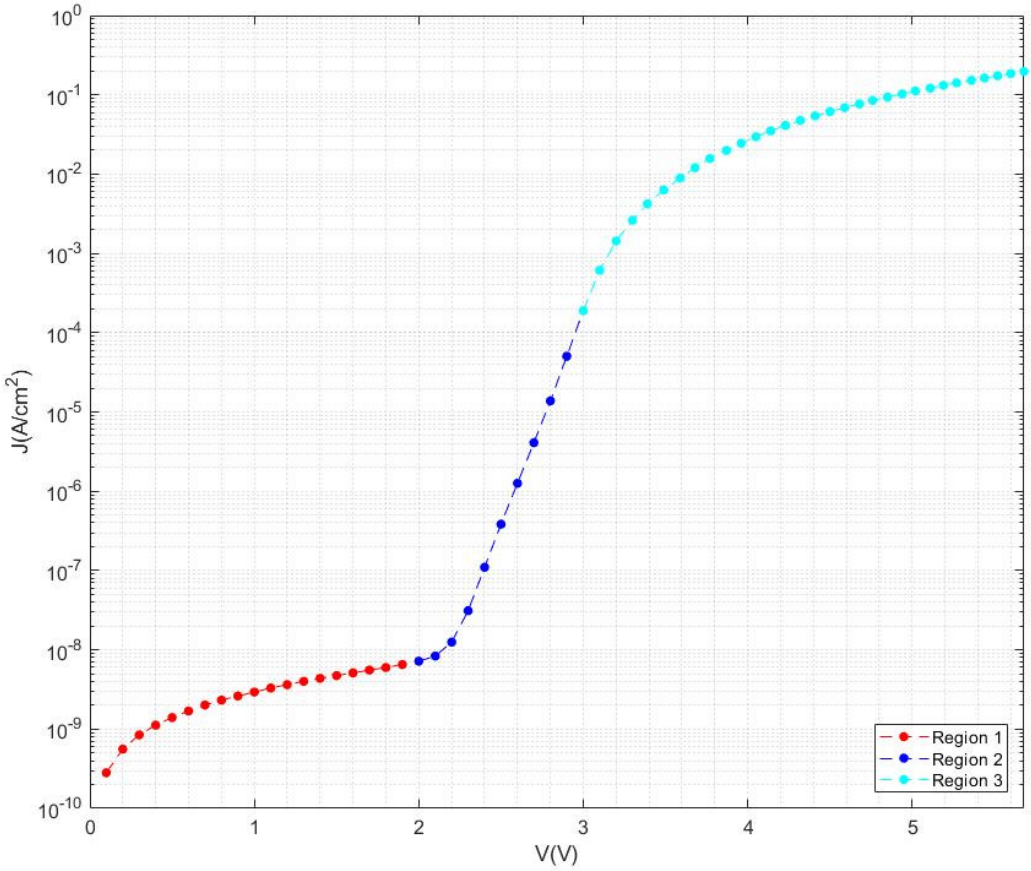


Figure 2-22 J-V characteristic curve of single unit OLED

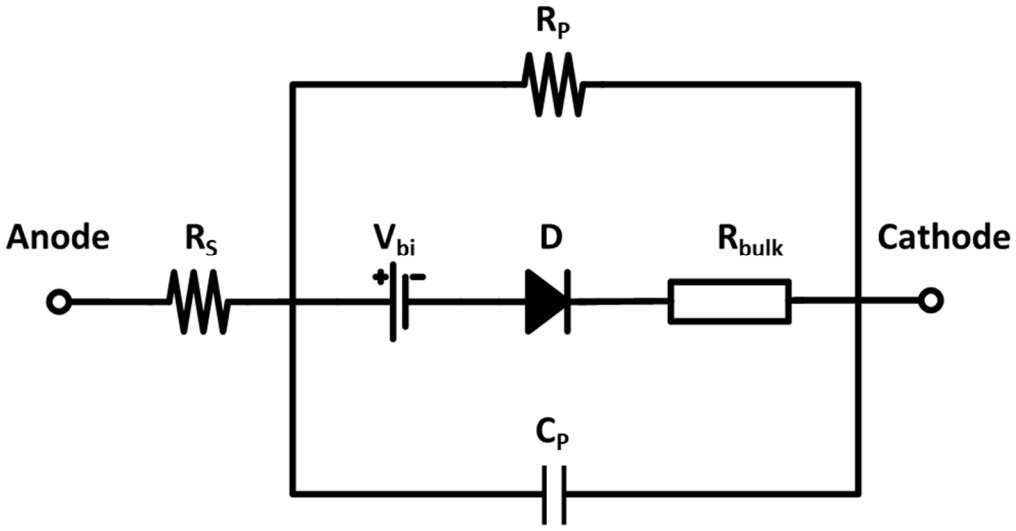


Figure 2-23 Single unit OLED SPICE model schematic

2.6.1 SPICE model components

2.6.1.1 Charge injection components – diode D, built-in voltage V_{bi}

It can be found from the J-V characteristics that there is a threshold voltage. The onset of exponential increase starts if the applied bias is higher than it. The threshold voltage is actually the built-in voltage V_{bi} describing the difference in the electric work function between the electrodes. The total injection of charge carriers from the contact electrode/organic heterojunction and the organic/organic junction is described by a simplified version of the Schottky Equation 2-2,

$$J_D = J_s[\exp\left(\frac{qV_D}{Nk_BT}\right) - 1] \qquad \textbf{Equation 2-23}$$

where J_S is the saturation current density, V_D is the voltage across the diode, N is the ideality factor, T is the thermal temperature.

2.6.1.2 Organic layer bulk control component – bulk resistor R_{bulk}

As discussed in Section 2.3.3, most of the previous proposed OLED SPICE models [132, 134] employed a linear resistor to represent the resistance of the organic layers. However, for organic materials, the combination of space charge MG equation, effects of trapping and the electric field dependent mobility lead to a power law increase. The J-V curve shows an analytical power law increase following the exponential growth. Hereby, we used a variable resistor element to describe the bulk limited mechanism,

$$J_{bulk} = K \cdot V_{bulk}^{m} \qquad \textbf{Equation 2-24}$$

It is difficult to precisely interpret the parameters K, m. Space charge limited current and trapped charge limited current might be the case. If the extracted value of m is 2 (or close to 2), SCLC is probably dominant (section 2.2.3.1). Otherwise, if m is higher than two, it is more likely to have traps appearance (section 2.2.3.2). However, as discussed in section 2.2.3, the constant mobility and the unipolar current assumption are not valid. Both SCLC and TCLC are not applicable to OLEDs.

Nonetheless, the power law J-V curve has been reported by several OLED studies [71, 140] before. Thus, we use the R_{bulk} to describing the power law characteristics. It provides information on the overall behavior of a multilayer structure. If consider OLED as an analogy to a single organic layer diode, the parameter K might link to the density of states, the carrier mobility and organic layer thickness and m is related to the density of states and the distribution of deep traps. Both K and m are determined by a mixture of effects of device physics.

Besides, the separation of the effects of the injection and the transportation of charges is only possible when the current of the structures is not limited by both injection and bulk (SCLC or TCLC). The use of doped layers creates quasi-ohmic contacts (intrinsic to positively doped, or intrinsic to negatively

doped) which limit the charge carriers. The currents in the multilayer PIN-OLED structures are more likely limited by the bulk, rather than charge injection.

2.6.1.3 Leakage current component R_P and contact resistance component R_S

A parallel resistor R_P is employed to approximate the leakage current for voltage bias less than V_{bi}. The value of R_P is related to he substrate surface roughness and the organic layer diffusion current.

R_s is the resistance of interconnections of the OLED device. It is negligible unless a very high current or high frequency is applied.

2.6.2 Modelling method

The MatLab polyfit function[10] and nonlinear regression model function[11] are employed. The linear resistor R_P is fit by the polyfit function. The nonlinear regression model extracts the parameters of D and R_{bulk}. For the nonlinear model, the current and voltage measurements are across a wide dynamic range; also, the impedance analyser uses different measurement ranges to take measurements. The measurement error is not constant across different ranges. Thus, we set a robust fitting option with 'bisquare' weight function. The regression process runs iteratively with the weighted function until the function value satisfies the termination tolerance. The level of fitness is evaluated by the coefficient of determination, denoted R^2, is defined as,

$$R^2 = 1 - \frac{SSR}{SST}$$

$$SST = \sum_i (y_i - \bar{y})^2 \qquad \textbf{Equation 2-25}$$

$$SSR = \sum_i (\hat{y}_i - \bar{y})^2$$

Where SST (total sum of squares) is the sum of squared deviations of the data values (y_i) from their mean ($\bar{y}$), SSR (regression sum of squares) is the sum of the fitted value ($\hat{y}_i$) from the mean of the data value ($\bar{y}$). Besides, we employ a p-value to evaluate the statistical significance of each parameter. It is computed through the comparison of the t-value, which is the standard deviation of the parameter, to the Student's t-distribution[12]. For example, if 95% of the t-distribution is closer to the mean than the t-value of the parameter, thereafter the p-value is 5%. The lower the p-value is, the higher the coefficient confidence level is.

[10] https://uk.mathworks.com/help/matlab/ref/polyfit.html
[11] https://uk.mathworks.com/help/stats/fitnlm.html
[12] https://uk.mathworks.com/help/stats/students-t-distribution.html

In order to obtain a good level of fitting, we extract the parameters according to the J-V curve region. Each of the components, representing a physical mechanism, is dominant at a certain voltage region. From 0 to 2V (Region Ⅰ), the J-V curve is at leakage current region. R_P is extracted through linear regression. In region Ⅱ, from 2V to 3V, the J-V curve increases exponentially. The injection-limited mechanism is dominant. We extract a group of initial value for the parameters of Diode D in this region. These parameter values are then input to fit the J-V curve at 3V to 6V (Region Ⅲ) where the curve starts to saturate into bulk-limited conduction. The parameters of both D and R_{bulk} are obtained from Equation 2-23 and Equation 2-24,

$$V(J) = V_{bi} + V_{bulk} + V_D$$

$$V_{bulk} = \left(\frac{J_{bulk}}{K}\right)^{1/m}$$

$$V_D = \frac{Nk_BT}{q}\log\left(\frac{J_D}{J_S} + 1\right)$$

Equation 2-26

$$V(J) = V_{bi} + \left(\frac{J}{K}\right)^{1/m} + \frac{Nk_BT}{q}\log\left(\frac{J}{J_S} + 1\right)$$

Where V_{bi}, K, m, $\frac{Nk_BT}{q}$, J_S are treat as parameters to be extracted.

2.6.3 Modelling result

Table 2-2 shows the value of the extracted parameters and the coefficient p-value. The R^2 value is 0.9999866 and adjusted R^2 is 0.9999854. A good level of fitting is obtained. Besides, the miniscule p-values of the coefficients indicate a high confidence level for each parameter.

Table 2-2 the value of the extracted parameters, and the p-value associated

Extracted parameters	Value	P-value
R_P (kΩ·cm^2)	331 477	4.7E-13
V_{bi} (V)	1.8152	1.4E-56
J_S (mA/cm^2)	2.167E-8	0
N	3.25	1.2E-44
K (mA/(cm^2·V^{-m}))	54.8	1.4E-38
m	1.61	4.6E-50

Figure 2-24 shows the fitting curve result in log scale (a) and linear scale (b). The model curve simulates the measurement curve precisely. The J-V plot of R_P (black) shows that it dominates the current density from 0 to about 2V. Thereafter, from 2V to 3V, apart from the built-in voltage, the applied bias is mostly dropped on the diode D. The current density increases exponentially. Then, with the applied bias higher than 3V, the influence of the bulk resistor R_{bulk} starts to grow.

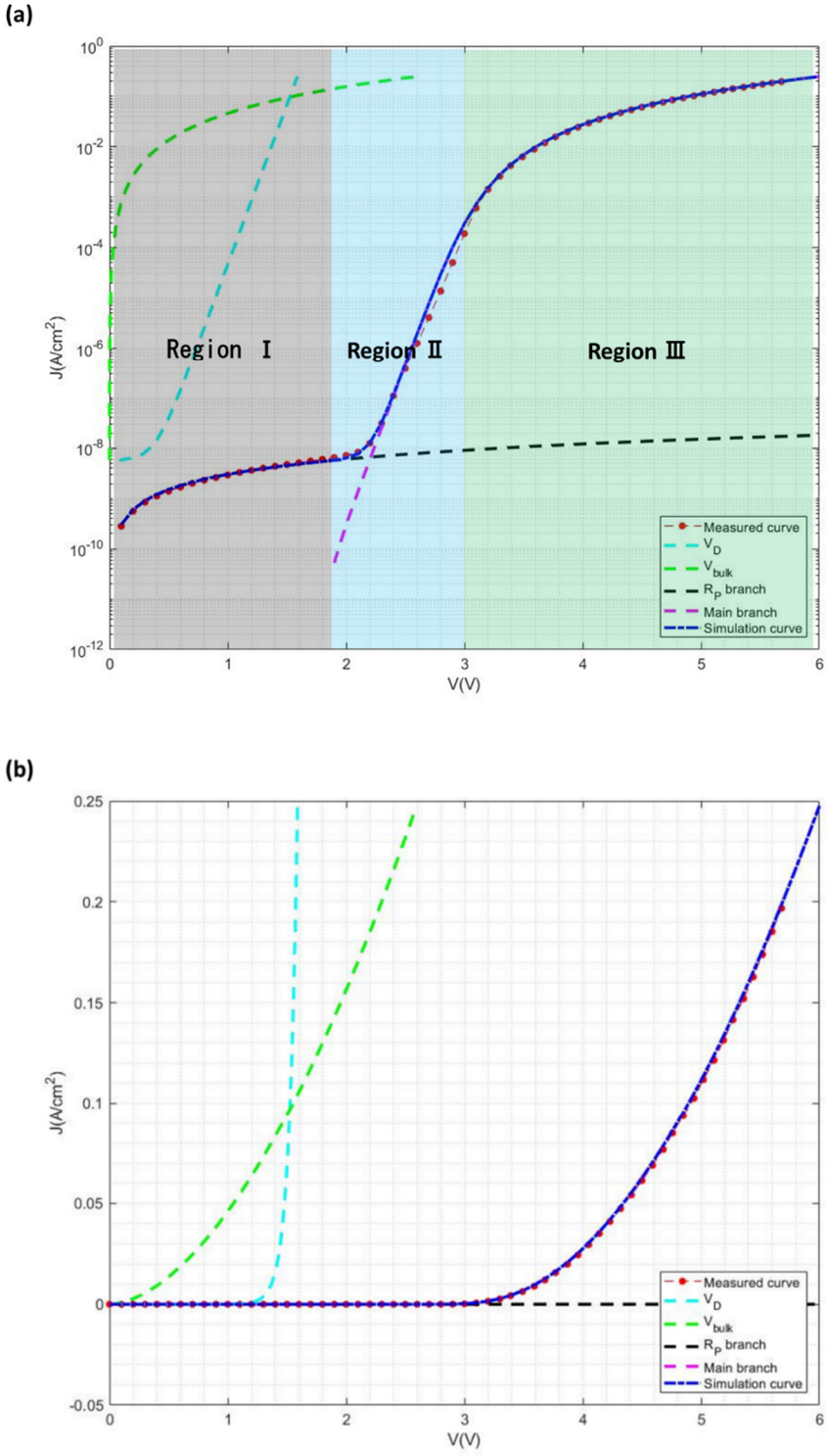


Figure 2-24 Comparison of the measured J-V curve (red dash, dotted line) and the simulation curve (blue dash line), the R_P branch current (black dash line), the main branch current (magenta dash line), the voltage on diode (cyan dash line), the voltage on R_{bulk} (green dash line) in y-axis log scale (a) and linear scale (b)

2.7 Tandem structure OLED SPICE model

2.7.1 Single unit and tandem structure OLED electrical characteristics

The measured steady-state J-V curves of both single unit (pink) and tandem structure (blue) OLEDs are shown in Figure 2-25. The tandem OLED samples are measured through a reproducibility test of the 27 samples shown in Figure 2-20. Average J-V of the 26 samples, with outliners removed, are taken for comparison.

Compared to the single unit OLED, the TOLEDs have a higher threshold voltage. The J-V curve starts exponential increase at around 4V (region 3), twice the threshold voltage of single unit OLED. The J-V curve then saturates to bulk-limited current following the exponential increase (region 4). The slope of the exponential increase is less than that of the single unit OLED. From 0 to 2V (region 1), the J-V curve increases linearly with a tiny slope similar to the single unit OLED leakage current. The J-V curve looks alike from 0 to 2V and 4V to higher values.

The distinctive region is at 2V to 4V (region 2) where the current start to increase but is not exponential as the case for the single unit OLED. One possible explanation is that one of the TOLED EL unit has a lower built-in voltage. It starts the exponential increase while the other unit is still in low leakage current region. The increase of the J-V curve is slow until the applied bias overcomes the built-in voltage of both units in the tandem structure. Thus, the current increases neither linearly nor exponentially in the bias region.

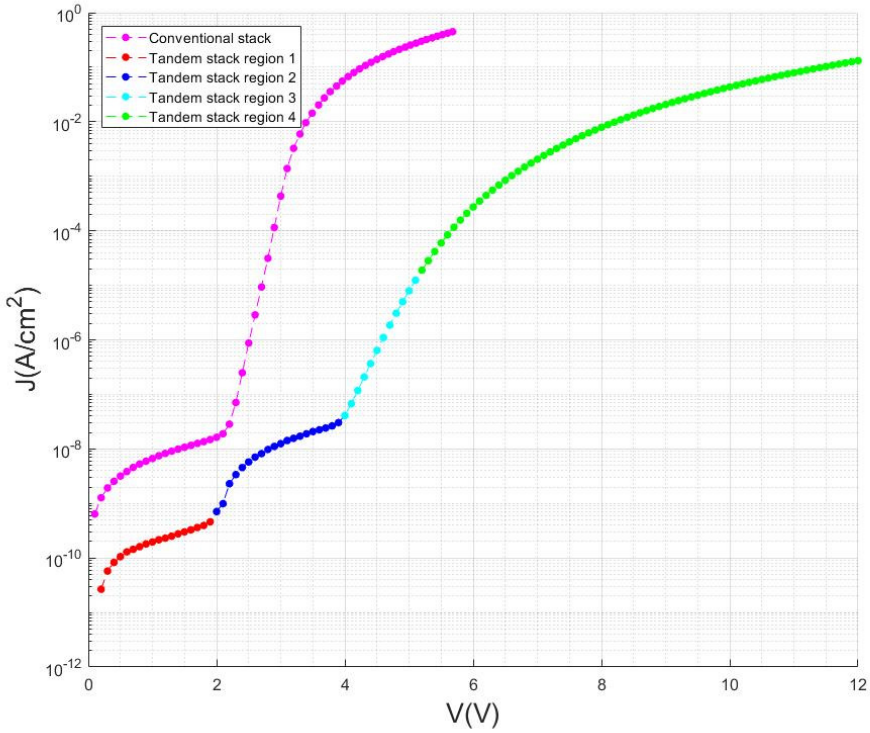


Figure 2-25 Comparison of DC J-V characteristics of conventional and tandem stack OLED

2.7.2 Two branch tandem SPICE model

The initial approach was SPICE model which cascades two conventional single emitting layer SPICE model as shown in Figure 2-26 (a). However, it is nearly impossible to obtain a reasonable curve fitting if there are two SPICE component in series with similar equations. One of the components will dominate and the other components' extracted parameters would have negligible effects on the J-V curve.

Thus, we make a hypothesis that one of the two EL diodes is turned on at a lower bias voltage than the other. In this case, there are three different working cases: both EL diodes are off; One EL diode is on, the other is off; both EL diodes turn on. In the J-V plot Figure 2-25, in region 1, which is showing the leakage current, both EL diodes are off. It can be modelled by a parallel resistor. In region 2, it shows a small increase in the J-V curve. We assume one EL diode is on while the other is still off in this region. In region 3 and 4, an exponential increases following by a bulk-limited characteristics are shown. It indicates both EL starts to conduct. In these two regions, the J-V characteristics can be described by the conventional single unit OLED model.

We modify the tandem OLED SPICE model into two branches. One branch starts conduction at a lower voltage. This branch does not necessary to have both D and R_{bulk}. As the exponential increase is dominant at region 2, where the bias voltage is low, we only employ D in this branch. And the second branch can be simplified to remove the diode D, as in region 3 and 4 both branches come into effect.

Therefore, the first branch, as shown 'L1' in Figure 2-26 (b), has a diode component and a built-in voltage V_{bi1}, describing the EL diode that turns at the lower volage. The second branch 'L2', has a bulk resistor and a built-in voltage V_{bi2}, describing the EL diode that turns on with higher applied voltage.

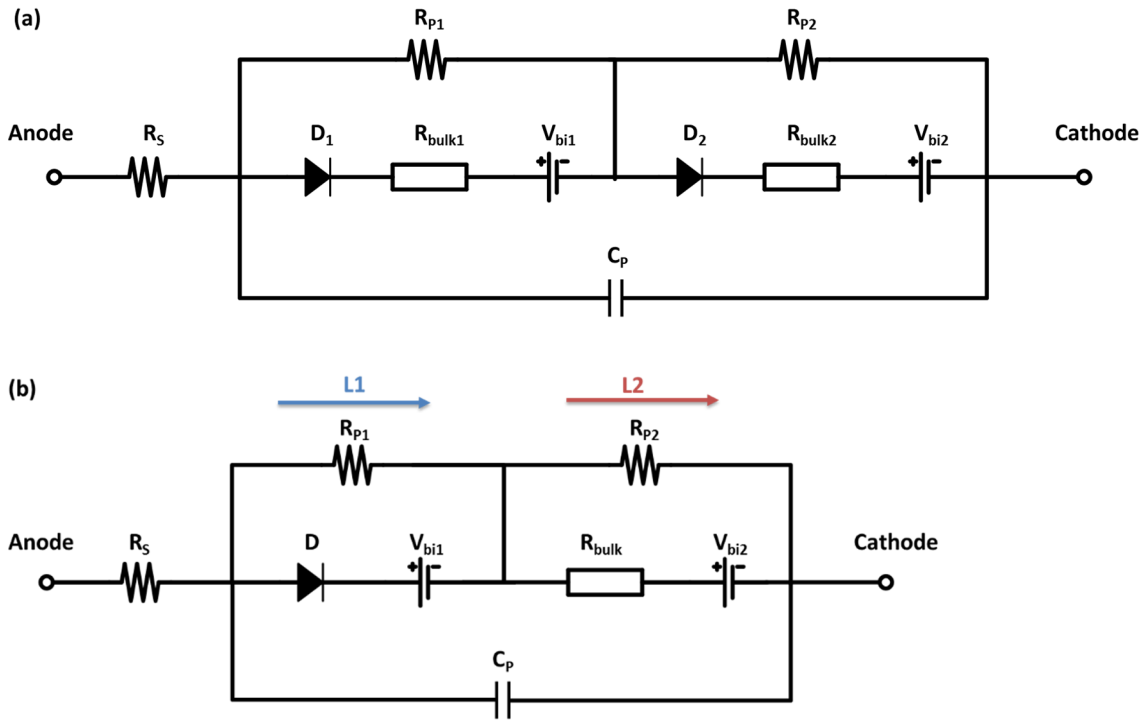


Figure 2-26 (a) initial series connection of two single unit OLED SPICE model; (b) simplified two branch model

2.7.3 Modelling method

We employ the same regression MatLab function as used for the single unit OLED SPICE model mentioned in section 2.7.3. Similarly, p-values are calculated to evaluate the confidence level of the extract parameters. Besides, we apply the nonlinear regression to the 26 tandem OLED samples. Analysis will be perform to the 26 sets of extracted parameters.

2.7.3.1 Steady-state response modelling

Similar to the single unit SPICE model, the components' parameters are extracted according to different bias voltage range. At voltage between 0 and 2V, the leakage current dominates, the sum of R_{p1} and R_{P2} can be extracted. For voltage from 5V to 12V, parameters of D (N, J_S), R_{bulk} (K, m), and the sum of built-in voltages (V_{bi1} + V_{bi2}) are extracted from Equation 2-26.

Thus, we acquire the parameters of D (N,J_S), R_{bulk}(K, m), and the sum of V_{bi} (V_{bi1} + V_{bi2}) and R_P (R_{P1}+R_{P2}). The parameters that need to resolved are the individual value of R_{P1}, R_{P2}, V_{bi1} and V_{bi2} from the J-V curve between 2V to 4V. According to the assumption made previously, only the diode is active

in this region. Figure 2-27 (a) shows the equivalent SPICE circuit model. However, there is no analytical solvable equation for curve fitting. The impedance of the diode D is based on an exponential (or log, if an equation of J) equation. R_{P1} and D are seen as parallel resistors, which are then in series with R_{P2}. There is no $J = f(V)$ (or $V = f(J)$) solutions available.

In order to resolve the equations, we further simplified the model to Figure 2-27 (b). The leakage resistor of diode branch, R_{P1}, is removed. The underlying assumption is that only a small amount of current will go through R_{P1}, the impedance of D is small compared to R_{P1} ($R_{p1} \gg \frac{\partial V_D}{\partial J_D}$). In this case, both the value V_{bi1} and R_{P2} are resolved by,

$$V(J) = V_{bi1} + J \cdot R_{P2} + \frac{N k_B T}{q} \log\left(\frac{J}{J_S} + 1\right)$$

Equation 2-27

The V_{bi2} and R_{P1} are then obtained through deduction of the total value.

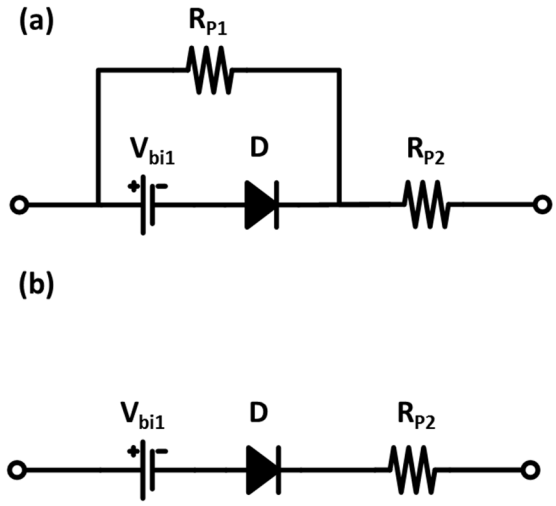


Figure 2-27 (a) Equivalent SPICE circuit model at voltage range between 2V to 4V; (b) simplified SPICE circuit for nonlinear regression in the voltage region

2.7.3.2 Transient/dynamic response modelling

The dynamic model is acquired through the AC small signal measurement. The main components to consider are the parallel capacitor C_P and series resistor R_S. R_S, representing the series connector impedance is ignored in the steady-state model for current density less than 100 mA/cm^2.

The impedance spectroscopy measurement is performed with a frequency range of 1kHz to 10MHz. The applied AC small signal is 10mV. A DC bias varied from 0 to 9V is applied. A 20s sweep delay is set between each measurement point.

The equivalent SPICE model for dynamic response is shown in Figure 2-28. R_{model} is the total impedance of the steady-state model. Equation 2-28 shows the equations to describe R_{model}. The small signal impedance of the diode (r_D) and the bulk-limited resistor (r_{bulk}) is derived from the slope of their J-V characteristics.

$$R_{model} = R_{p1} // r_D + R_{P2} // r_{bulk}$$

$$\frac{1}{r_D} = \frac{\partial J_D}{\partial V_D}\Big|_{V=V_{DC}} = \frac{q}{Nk_BT} J_S \exp\left(\frac{qV_D}{Nk_BT}\right) = \frac{q}{Nk_BT}(J_D + J_S)$$

$$\frac{1}{r_{bulk}} = \frac{\partial J_{bulk}}{\partial V_{bulk}}\Big|_{V=V_{DC}} = m \cdot K \cdot V_{bulk}^{m-1} = K^{\frac{1}{m}} \cdot m \cdot J_{bulk}^{\left(1-\frac{1}{m}\right)} \quad \textbf{Equation 2-28}$$

$$R_{model} = \frac{R_{p1}}{\frac{q}{Nk_BT}(J_D + J_S) \cdot R_{p1} + 1} + \frac{R_{p2}}{K^{\frac{1}{m}} \cdot m \cdot J_{bulk}^{\left(1-\frac{1}{m}\right)} \cdot R_{p2} + 1}$$

The double slash (//) symbol represent parallel, the equivalent impedance of the two impedance are combined in parallel. r_D is the small signal impedance of the Schottky diode, which is derivation of

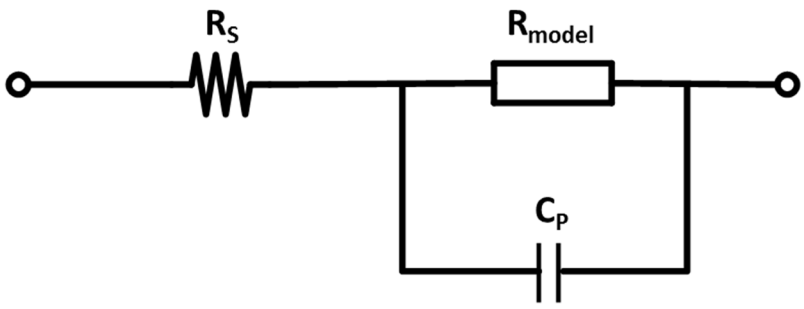


Figure 2-28 equivalent circuit diagram for the dynamic response, R_{model} is the total impedance of the steady-state model

The AC measurement returns a complex impedance Z at certain DC bias and frequency. The real and imaginary part can be represented as,

$$Z = R_s + R_{model} \,//\, \frac{1}{i\omega C} = \Re + i\Im$$

$$\Re = R_s + \frac{R_{model}}{1 + R_{model}^2 C^2 \omega^2}$$

$$\Im = -\frac{R_{model}^2 C\omega}{1 + R_{model}^2 C^2 \omega^2}$$

$$\omega = 2\pi f$$

Equation 2-29

We employ the Zfit function[13] based in MatLab to resolve the equations to extract C_P, R_S. It fits the impedance spectroscopy data via the fminsearch function[14], which searches the minimum distance to the experimental data points with varying parameters. The calculated R_{model} is input as a fixed value parameter. C_P, R_S are extracted through the fminsearch function.

In order to estimate the impedance of the dynamic model, we applied an AC domain simulation for different value of R_{model} (equivalent to different DC bias for the tandem OLED). The other component are fixed to typical values (assume for a 0.44cm^2 sample), R_S = 100Ω, C_P = 10nF. As shown in Figure 2-29 (a), there are two plateaus for the magnitude of impedance. For low frequency, the impedance is equivalent to R_S + R_{model}, considering the C_P as open-circuit. For high frequency, the impedance becomes R_S, as the impedance of C_P is small. Similar to the other RC filter circuits, there is a cut-off frequency indicating the $\frac{1}{\sqrt{2}}$ point, also known as characteristic relaxation frequency f_r in terms of a dielectric material. The relaxation frequency is calculated to be $2\pi R_{model} C_P$, which is related to the relaxation time $\tau_r = R_{model} C_P$. The phase of the modelled circuit also respond similarly to a typical RC filter. At the relaxation frequency point, the phase is shifted -45°. The phase shift is then increase to 0° as R_S begins to dominate the Z impedance. A U-shape phase plot is shown.

[13] https://uk.mathworks.com/matlabcentral/fileexchange/19460-zfit
[14] https://uk.mathworks.com/help/matlab/ref/fminsearch.html

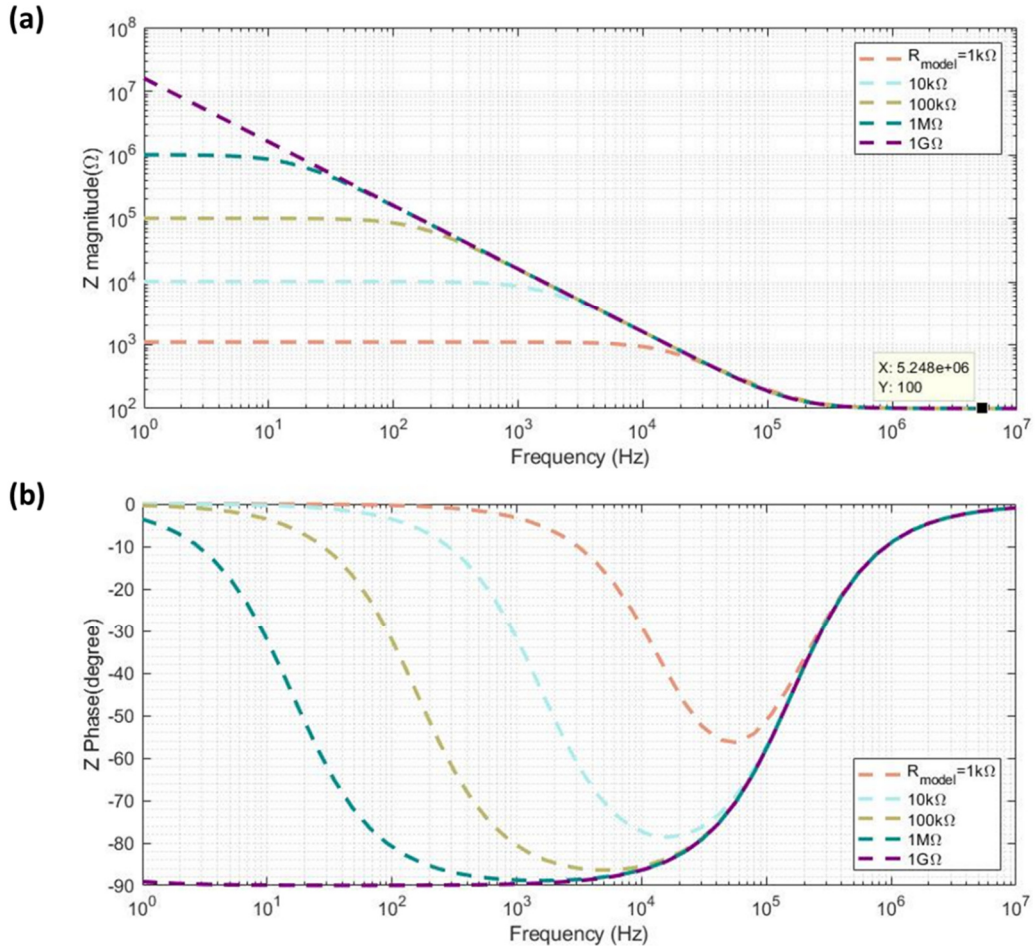


Figure 2-29 Impedance spectroscopy simulation of the RC circuit with R_S = 100Ω, C_P = 10nF, R_{model} = 1kΩ, 10kΩ, 100kΩ, 1MΩ and 1GΩ

2.7.4 Modelling result

2.7.4.1 Steady state response model result

We perform the parameter extractions for the 26 identical TOLED devices on the same wafer. First, we acquired a group of parameters that fit the average J-V curve of the 26 samples. The parameters' values are shown in column 2 of Table 2-3. Figure 2-30 shows the comparison of simulated J-V curve (blue dash line) and the average J-V curve plot (red dot dash line). Good level of agreement is achieved. There is only small mismatch at 1.8V to 2.3V. The cause of the mismatch could be the neglect of the R_{P1}. In the light blue region of Figure 2-30 (a) where the R_{bulk} branch is ignored, the impedance is defined as,

$$R_{model} = R_{P2} + R_{P1}//R_D$$

Equation 2-30

Where R_D is the equivalent large signal impedance of the Schottky diode, described by Equation 2-30. However, when we perform linear regression, R_{P1} is ignored. The impedance is described as,

$$R_{regression} = R_{P2} + R_D \qquad \textbf{Equation 2-31}$$

The equivalent impedance R_D will be larger than $R_D//R_{P1}$. Thus, the extracted R_{P2} is with a smaller value from $R_{regression}$. The simulated current density will be higher than the experimental. The issue is serious when the voltage bias is small, the assumption $R_D << R_{P1}$ is not valid. Therefore, there is a noticeable difference at relative low voltage (1.8V to 2.3V), but not other voltage range.

We can make a comparison of the value of the extracted parameters from the single-unit OLED and TOLEDs. The leakage resistors of TOLED ($R_{P1}+R_{P2}$=4.9 GΩ·cm^2) are higher than the single-unit OLED (R_P=331 MΩ·cm^2) which indicates the lower leakage current shown in Figure 2-25. For the built-in voltage, the TOLED built-in voltage ($V_{bi1}+V_{bi2}$=2.8V) is higher than the single-unit's (V_{bi}=1.8V). However, it is not the doubled number as expected. The reason could be the turn-on of the diode branch at 2V to 4V, which introduces voltage across the diode before the OLED is fully turned on. For the diode parameters, the saturation current density J_S of TOLED (1.8E-8 mA/cm^2) is slightly smaller than that of the single-unit OLED (2.1E-8 mA/cm^2), and the ideality factor N of TOLED (5.96) is almost double of the single unit OLED's (3.25). Considering the voltage region that the diode component is dominant, the ideality factor is reflecting the slope of the exponential increase region. According to Equation 2-30, the higher N and smaller J_S are, the less the slope of exponential increase is. This makes sense with the parameter values, as the single-unit OLED is with a higher slope of exponential increase. For the R_{bulk} parameters, K of single-unit OLED (54.8 mA/(cm^2·V^{-m})) is much higher than the TOLED's (0.9 mA/(cm^2·V^{-m})), and the exponent m is 1.8 for single unit and 2.9 for TOLED. The parameter K is influenced by multiple factors. But considering the exponent m, the TOLED has a higher m value which shows in the J-V curve that it is saturated with a larger slope in a log plot.

Besides, parameter extractions are also performed to each of the 26 tandem OLED samples. The manufacturing process variation of the OLED can be monitored through the parameters.The mean (μ), standard deviation (σ) and normalised standard deviation (σ/μ) of the parameters are shown in Table 2-3. The normalised standard deviation of most parameters is found to be less than 5%. Only the leakage resistor R_{P1}, R_{P2} and K are higher. The variation of R_{P1}, R_{P2} can be induced from the hysteresis effect mismatch between OLEDs. We applied same delay time – 10s for all samples, but the hysteresis might be different from sample to sample.

Table 2-3 Extracted parameter values, from the mean J-V curve (second column), the mean values from extractions of multiple samples (third column), the standard deviation from extractions of multiple samples (fourth column), and normalised standard deviation (fifth column).

Extracted parameters	Values from Mean J-V	Mean of multiple samples (μ)	Standard deviation (σ)	Normalised SD (σ/μ)
R_{P1} (kΩ·cm^2)	4.8515E6	4.8662E6	3.3749E5	6.9%
R_{P2} (kΩ·cm^2)	52 947	58 679	19 803	33.7%
V_{bi1} (V)	1.317	1.3237	0.0653	4.9%
V_{bi2} (V)	1.4868	1.5014	0.0602	4%
J_S (mA/cm^2)	1.7861E-8	1.7784E-8	1.8302E-10	1%
N	5.96	5.874	0.1163	1.9%
K (mA/(cm^2·V^{-m}))	0.9136	0.8754	0.07646	8.7%
m	2.8555	2.8768	0.0319	1.1%

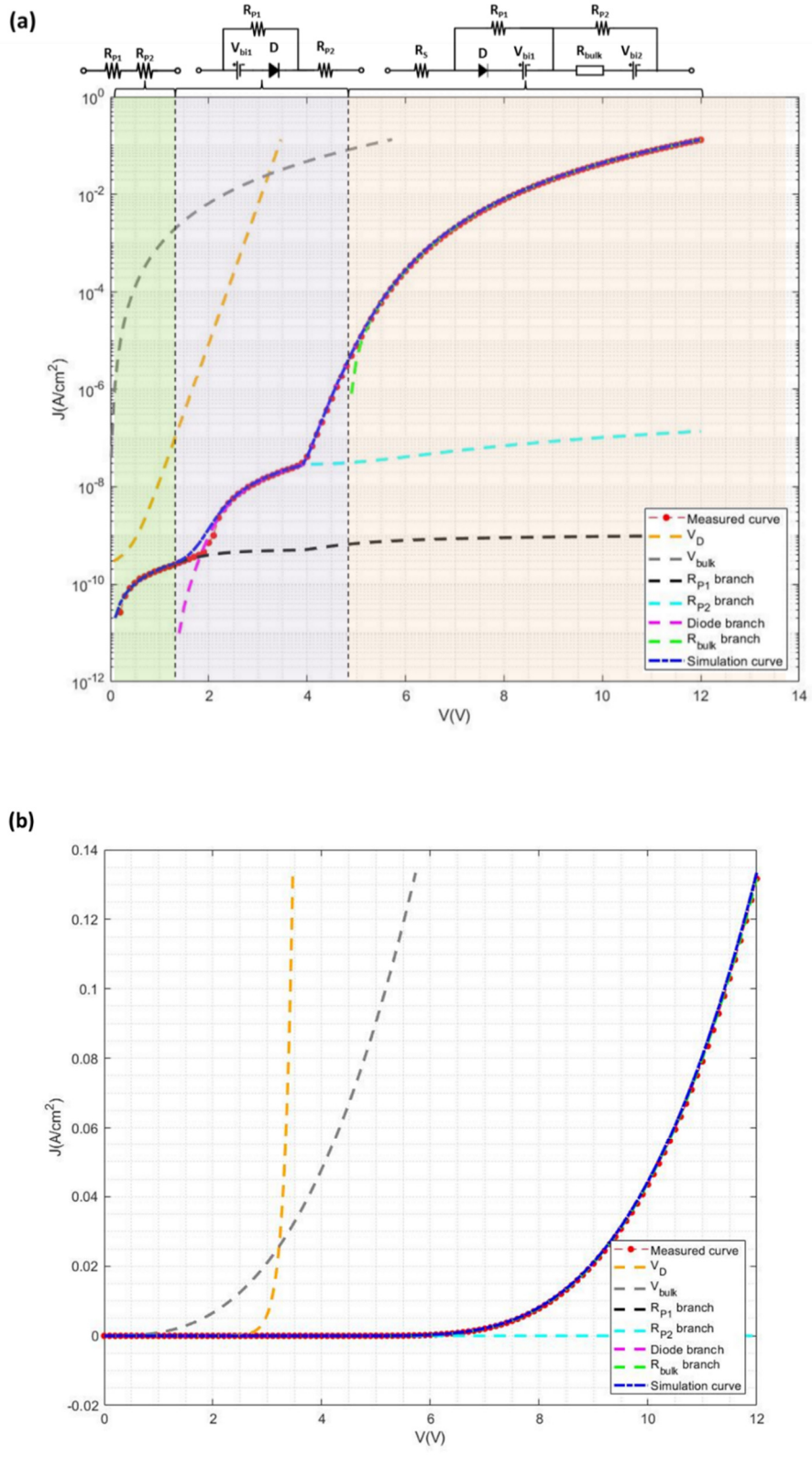


Figure 2-30 the measured and modelled J-V characteristic curves in (a) log scale y-axis and (b) linear scale y-axis, the J-V curves of each component (Schottky diode, bulk resistor, R_{P1}, R_{P2} are included) are plotted

2.7.4.2 Dynamic response model result

The absolute magnitude (|Z|) and phase (θ) of the impedance versus frequency with bias varied from 1V to 9V are plotted in Figure 2-31. Over frequency range from 1kHz to 0.4MHz, the impedance spectroscopy is with similar shape to the simulation's in Figure 2-29. The impedance shows linear decay (log x-axis) for small voltage bias (≤5V). The DC model resistor is with relative high value in these voltage biases, R_{model} = 8.14GΩ (1V), 137MΩ (3V), 32.7kΩ (5V), which caused the relaxation frequency is less than 1kHz (the lower bound of measured frequency range). For bias of 7V and 9V, the Z magnitude starts from a relative constant level at low frequency and decay at the relaxation frequency. The Z phase is also similar to the simulation's with a U-shape response.

However, a rise of Z magnitude and positive phase appears at high frequencies (≈0.4Mhz). It can be caused by either an occurrence of negative capacitance or the inductance of the lead cables. Ehrenfreund et al. [141] have previously reported appearance negative capacitance in OLEDs. They found negative capacitance appeared at low frequencies induced by charge carrier recombination. But the positive phase we measured is at high frequencies and bias less than V_{bi} (very few recombination). Therefore, it is likely that the lead cable inductance is the main cause. S. Nowy [142] have shown the effect of cables' inductance in OLED impedance spectroscopy measurements. In order to minimise the inductance influences, the high frequency measurement points (≥0.4MHz) are ignored for C_P and R_S extraction.

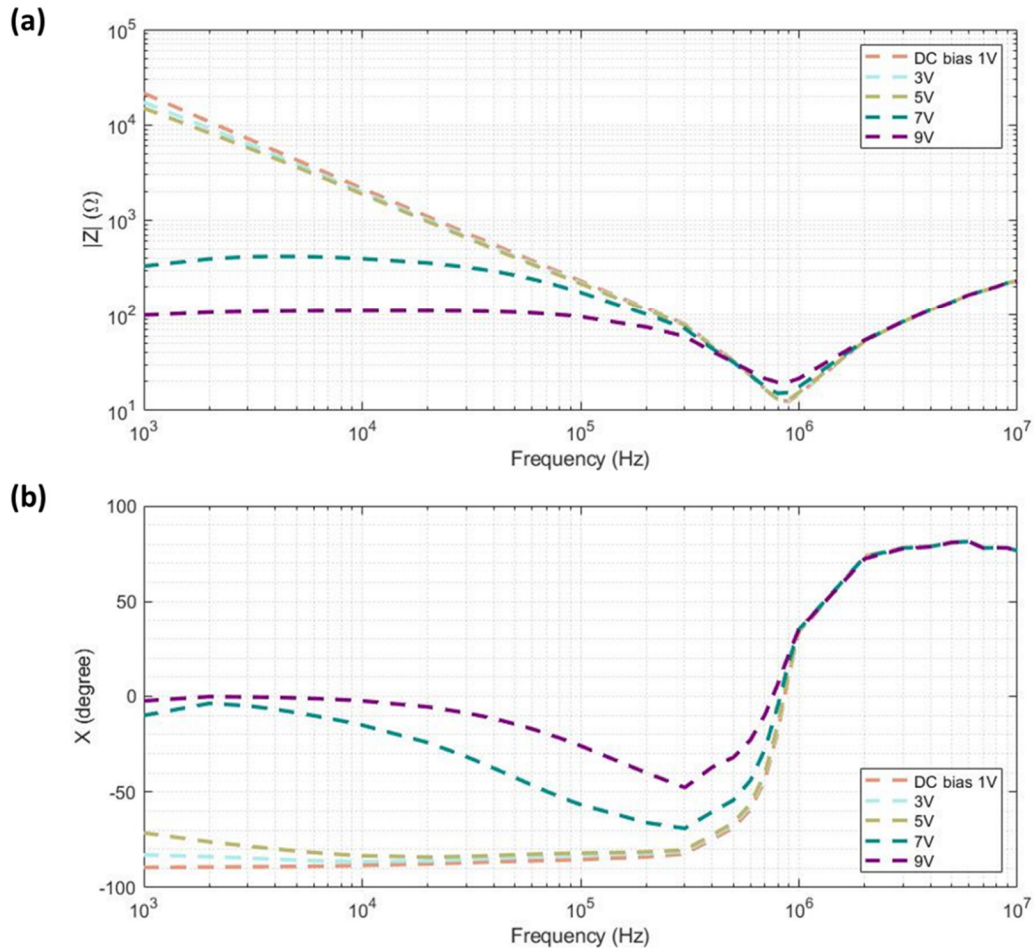


Figure 2-31 (a) Impedance magnitude and (b) phase spectra of the tandem OLED at bias between 1V and 9V

The extracted value of C_P and R_S versus different biases are shown in Figure 2-32. Both C_P and R_S do vary with different DC biases. But there is not with a big variation between them. The average of C_P is 22 nF, with a standard deviation of 1.5nF, normalised to be 7%. The average of R_S is 7.5Ω, accompanied by a standard deviation of 0.7Ω, normalised to be 9%. The mean value of both C_P and R_S across various DC bias are taken. The plot of the modelled result comparing experimental is shown in Figure 2-33. The modelled impedance magnitude and phase are in good agreement with measured values over 1kHz to 0.3MHz.

The measured curves deviate from the AC simulated curves in Figure 2-29 at high frequency (>1 MHz). As we discussed above, the appearance of increased impedance and positive phase at high frequencies is likely to ascribe to the lead cables of the measurement setup. The high frequency inductance could suggest a second resonance. Previous publications have employed a non-constant capacitance to model the AC response in OLEDs [54, 142, 143]. It requires to take account of each OLED layer and more SPICE components (capacitors, resistors or constant phase element) to realize a more accurate model.

Besides, it is unlikely for the analogue PWM pixel presented in (section 3.5.2) to drive the OLED at MHz. Thus, the high deviations at high frequency are neglected in the model.

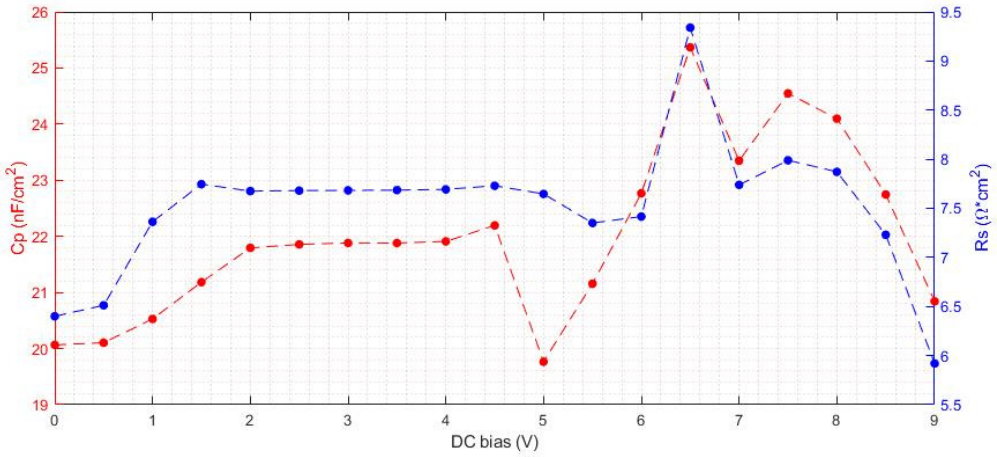


Figure 2-32 Plots of the extracted value for C_P (left y-axis) and R_S (right y-axis)

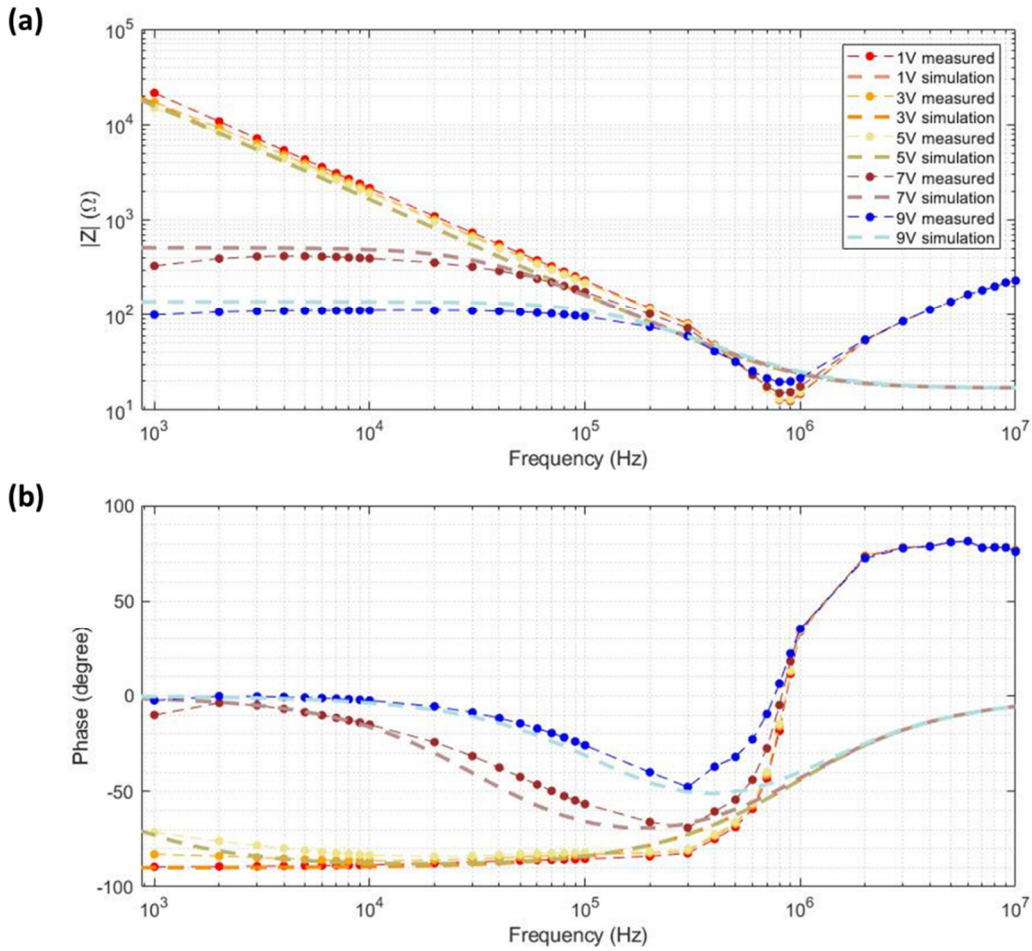


Figure 2-33 comparison of the measured and model simulated impedance spectroscopy (a) magnitude and (b) phase with different DC biases. Plot (b) has the same legend as plot (a)

2.7.5 Electron transport layer and charge generation layer effect on the model

We have demonstrated extracting parameters from multiple OLED samples with the same structure and materials to effectively detect any die-to-die variations. In order to further investigate the physical meaning of each component, we have performed modelling of multiple tandem OLEDs employing different types of materials. As shown in Table 2-4, there are four types of different OLEDs. Two different types of electron transport layer (ETL) and two different types charge generation layer (CGL) are used.

The J-V characteristic curves of these four samples and their simulation curves are plotted in Figure 2-34. At bias from 2V to 4V, sample 1 and sample 2 have similar low voltage characteristics, which is a higher leakage current, compared to sample 3 and sample 4. The different CGL material can be the cause of a different leakage current. On the other hand, at high voltages (>5V), sample 1 and sample 3 have similar J-V curve, while the current of sample 2 and sample 4 are less. The reason can be the ETL material inducing different bulk-limited current.

The model allows a good level of fitting to all of these samples. The extracted parameters are shown in Table 2-5. It can be found that, with the same CGL, the parameters relating to the low voltage response (R_{P1}, R_{P2}, V_{bi1}, V_{bi2}) are with similar values (sample 1 & sample 2, sample 3 & sample 4). Besides, the parameters of bulk-limited component R_{bulk} (K, m) are relevant to the ETL, which sample 1 and sample 3 are similar, while they are different from sample 2 and sample 4. For the parameters of the diode component, which is describing the exponential increase region, they vary from the different samples. It is likely caused by the different characteristics of the intermediate transition region (from low voltage to high voltage) where the diode component is dominate.

Table 2-4 Four test OLED with different types of ETL and CGL materials

	ETL1	ELT2
CGL1	Sample 1	Sample 2
CGL2	Sample 3	Sample 4

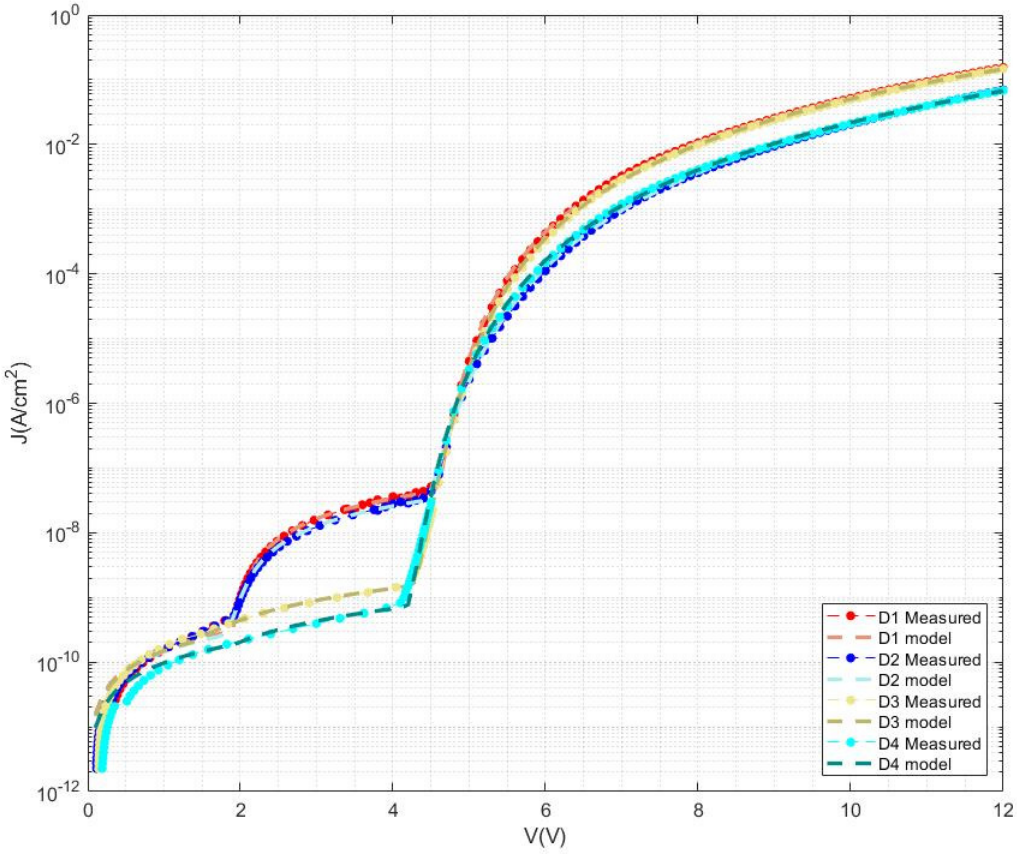


Figure 2-34 The J-V characteristic curves of sample 1 (D1), sample 2 (D2), sample 3 (D3) and sample 4 (D4) and their modelled curves

Table 2-5 The extracted parameters these four OLEDs

Extracted parameters	Sample 1	Sample 2	Sample 3	Sample 4
R_{P1} (kΩ·cm²)	6.25E6	6.83E6	4.6592E6	6.19E6
R_{P2} (kΩ·cm²)	55 975	71 913	2.0477E6	4.0738E6
V_{bi1} (V)	1.8616	1.7677	0.96471	1.1454
V_{bi2} (V)	2.4363	2.2459	3.08279	2.9033
J_S (mA/cm^2)	4.47E-8	4.47E-8	3.91E-8	4.46E-8
N	1.44	2.28	2.59	2.04
K (mA/(cm^2·V^{-m}))	0.32	0.083	0.505	0.097
m	3.2	3.52	3.03	3.4

2.8 Summary and Conclusions

In this chapter, a novel SPICE model for TOLED is introduced. The electrical characteristics of both single-unit and tandem structure OLEDs are discussed. Both DC steady-state response and AC dynamic response matches the SPICE simulations with negligible error.

Table 2-6 shows a comparison between the TOLED SPICE model in this work and other published OLED SPICE models. As the TOLED SPICE model is based theoretical OLED model equations and avoid using piece-wise curve fitting, the model would be feasible to other types of TOLED with different layer materials (such as ETL, CGL shown in section 2.7.5).

Table 2-6 Comparison table of OLED SPICE model from this work and other publications

Author	This work	Li [134]	Kanicki [135]	Pinot [75]	Buso [72]	V.Bender [74]	Lin [136]
Year		2005	2005	2008	2014	2015	2016
Single / Tandem	Tandem	Single					
AC/dynamic response	✓	✗	✓	✓	✓	✓	✓
Number of components	8	3	8	6	6	11	4
Model components/ equations	bulk resistor + RS diode	SCLC resistor	Piece-wise curve fitting[15]	bulk resistor + RS diode	Exponential diode + nonlinear resistor	Piece-wise curve fitting[16]	Shockley + MG piece-wise curve

The next chapter discusses the application of the TOLED SPICE model for the circuit design and simulation in search for a scalable pixel design to attain a high performance TOLED microdisplay pixel.

[15] Three equations including FN tunnelling, SCLC and n>2 power law are used
[16] Fit by resistor linear equations

3 Pixel circuit design for tandem structure OLEDs

3.1 Introduction

The first part of this chapter provides a review of OLED microdisplay circuits. A number of published designs are considered: analogue constant voltage driving, analogue current programmed current driving, analogue voltage programmed current driving, analogue compensation scheme pixel, digital PWM (pulse width modulation) pixel and analogue PWM pixel. As discussed in Chapter 2, tandem structure OLED is an emerging type of OLED device which provides high quantum efficiency and long lifetime. The challenge for TOLED driver design is the high drive voltage and the resulting wide voltage dynamic range. In the second part of this chapter, several pixel designs that have been proposed and implemented to drive TOLED are analysed and characterised. A conclusion is made to compare the performance among these pixels.

3.2 OLED pixel architecture

The pixel architecture design of CMOS-based OLED microdisplay is driven from the development of reflective LCoS microdisplay since the 1990s. In LCoS, a liquid crystal layer is deposited between an array of pixel electrodes and a transparent indium-tin-oxide (ITO) counter electrode. A voltage is applied to switch the polarized light. On the other hand, for OLED microdisplays, a stack of organic layers are deposited between the pixel electrodes and the ITO counter electrodes. The OLED emission is controlled by a drive current or a voltage.

An example of the OLED microdisplay sub-pixel cross-section is shown schematically in Figure 3-1. The CMOS silicon act as a substrate for the OLED stack. The metal plate (ALU-CAP) electrode has several functions: it is the pixel electrode which drives the OLED stack; the reflective nature makes most of the emission light output through the top surface; last, it minimizes the exposure of the CMOS circuits to emission light which could induce photoelectrons. The ALU-CAP plate is required to be as large as the CMOS process design rule[17] allows reducing the gap between each metal plate. Moreover, the gap should be covered by the lower metal layers. Routing on the top metal layer also needs to be avoided which could be a challenge to the vintage single-metal silicon processes [5, 144]. The opaque substrate and the transmissive ITO electrode make it ideal for implementation of the top-emitting OLED stack. However, it is more challenge to make top-emitting OLED than the conventional bottom emission [145]. RGB colour filters are placed on top of the OLED after the thin film encapsulation to achieve full-colour emission. However, less than 1/3 of the overall luminance of the OLED is transmitted which reduces the efficiency. Thus, direct patterned RGB emitters is benefitial for OLED microdisplay. In 2016, Ghosh et al. [44] from eMagin demonstrated the first OLED microdisplay that directly patterned

[17] Design rules of CMOS processes are a set of geometrical specifications that dictate the design of the layout.

individual side-by-side red, green and blue OLED emitters and the reported luminance is up to 5000 cd/m^2 (< 2000 cd/m^2 for typical state-of-the-art full-colour OLED microdisplays).

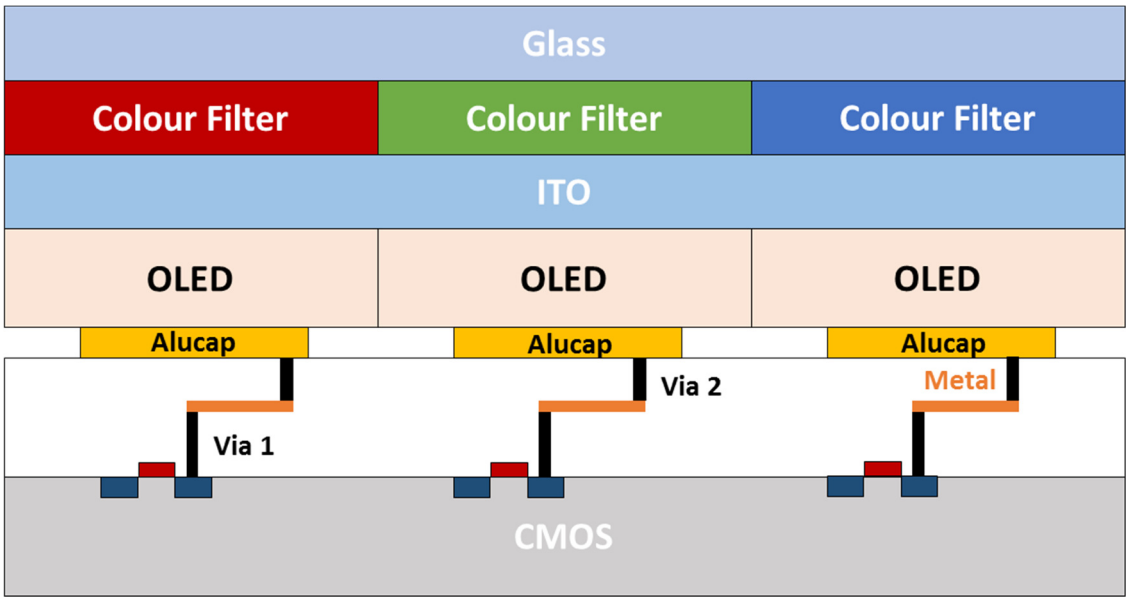


Figure 3-1 Schematic cross-section of OLED microdisplay pixel

3.3 State-of-the-art OLED Microdisplay Devices Survey

Table 3-1 summaries the specification of several OLED microdisplays published recently by the main microdisplay manufacturers. Ghosh et al. (eMagin) reported a 2048×2048, 9.3 µm pitch (sub-pixel pitch 3.5×3.35 µm^2 for red/green, two 3.3×7.85 µm^2 for blue) OLED microdisplay with a maximum luminance of 5000 cd/m^2 [44]. Wartenberg et al. reported on the LOMID (Large, cost-effective OLED microdisplays and their applications) project to develop a 1920×1200×4 OLED microdisplay [47]. Choi et al. (Kopin) demonstrated their Lightning OLED Microdisplay with a 2048×2048 resolution, 2.88 ×8.64 µm^2 sub-pixel pitch [28]. Haas et al. (MicroOLED) reported about a 0.39-inch XGA display with a pixel pitch of 7.6 µm (3342 ppi) with a sub-pixel pitch of 3.8 µm (4 sub-pixels per pixel) in an RGBW arrangement, and an SXGA display with 9.4 µm pixel pitch and a brightness of 3000 cd/m² in full color [43]. Fujii et al. (Sony) announced the world's smallest pixel pitch OLED microdisplay – 6.3µm [48, 49].

In general, a pixel pitch of around 10µm (subpixel area of 20~30µm^2), display resolution up to 2K and luminance level upto 5000 cd/m^2 are achieved in the state-of-the-art OLED microdisplays.

Table 3-1 OLED Microdisplay Specifications

Publication	eMagin [44]	Kopin [28]	MicroOLED [43]	LOMID [47]	Sony [49]
Year	2017	2017	2017	2018	2018
Array size	2048×2048×3	2048×2048×3	1024×768×4	1920×1200×4	1600×1200×3
Pixel/Sub-pixel pitch	9.3 µm	2.88 ×8.64 μm^2 sub-pixel	7.6 µm	11 µm	6.3 µm
Luminance	5000 cd/m^2	Not known	3000 cd/m^2	1500 cd/m^2	2000 cd/m^2
Pixel driver	4T1C pixel driver	Not known	Not known	Not known	Analog current drive with V_T compensation

3.4 OLED microdisplay pixel circuit review

In order to develop a microdisplay pixel to drive TOLED which also meets the state of the art specifications, we will start from a brief review of the pixel circuit that has been employed in previous designs. This section is not a complete or encyclopedic literature review. The interested readers can refer to the SID Introduction to Microdisplays [146] and the Handbook of Visual Display Technology [147] for further information. Although the review focuses on OLED microdisplay pixel design, some LCoS microdisplay pixel circuits are also considered, as both have a similar architecture regardless of the slightly different driving schemes.

3.4.1 Historical pixel design and classification

The microdisplay pixel circuits can be classified by the driving schemes as follow: a) Analogue Pixel Circuits; b) Digital PWM Pixel Circuits; c) Analogue PWM Pixel Circuits.

a) Analogue Pixel Circuits

The microdisplay pixel, which uses an analogue signal as input and converts the analogue signal to the analogue OLED luminance level, is a so-called analogue pixel. Figure 3-7 (b) shows the method of generating grayscale for the analogue pixel. There are mainly three analogue pixel approaches: 1) constant voltage driving method [26], 2) current programmed current driving method [30] and 3) voltage programmed current driving method [148].

For a constant voltage driver as in Figure 3-2, the drive MOSFET (MN2) is configured as a source follower operating in the saturation region. Good linearity is achieved as the OLED is driven by V_{DATA}-V_{th}[18]. The flicker level is low compared to the current driving method. The OLED voltage dynamic is from ~0 (ground) to VDD-V_{th}. However, the effect of the ageing of OLED makes the luminance decay faster. Moreover, the output OLED anode voltage is sensitive to the variation of V_{th}.

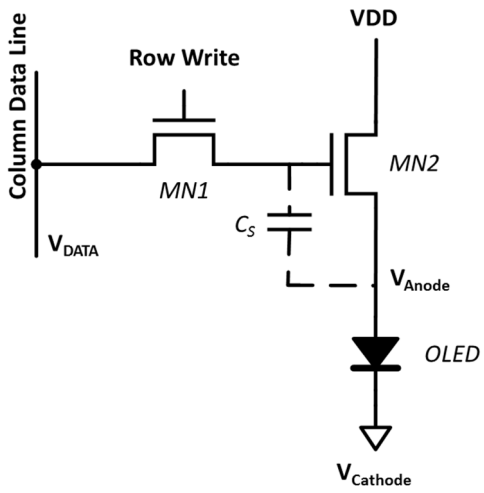


Figure 3-2 Constant voltage driving pixel circuit schematic

An example pixel circuit for the current programmed current driving method is shown Figure 3-3 [30]. The current I_{DATA} is copied to flow to the OLED. As the subpixel area is small, the small drive current biases the drive MOSFET in the subthreshold region [30]. In order to improve the current program stage, a fixed offset between V_{BH} and V_{BL} is applied. V_{BH} and V_{BL} have a voltage difference of $\zeta V_T/\ln(100)$[19] to change the subthreshold current by 100 times. V_B is at low voltage level V_{BL} for programming phase. For emitting phase, V_B is switched to a higher reference V_{BH} to scale the current down by a factor of 100.

Good uniformity is obtained without any influence of the mobility or V_{th} variation. The current driver has a relatively consistent luminance as the OLED is ageing. By scaling the programmed voltage, it is able to mitigate the problem of long programming time in low brightness. However, the scaling factor $\zeta V_T/\ln(100)$ could lead to pixel to pixel current mismatch.

[18] The threshold voltage suffers from body effect. It is bulk bias enhanced.
[19] According to the MOSFET subthreshold current Equation 3-7, ζ is a nonlinerity factor, V_T is the thermal voltage kT/q.

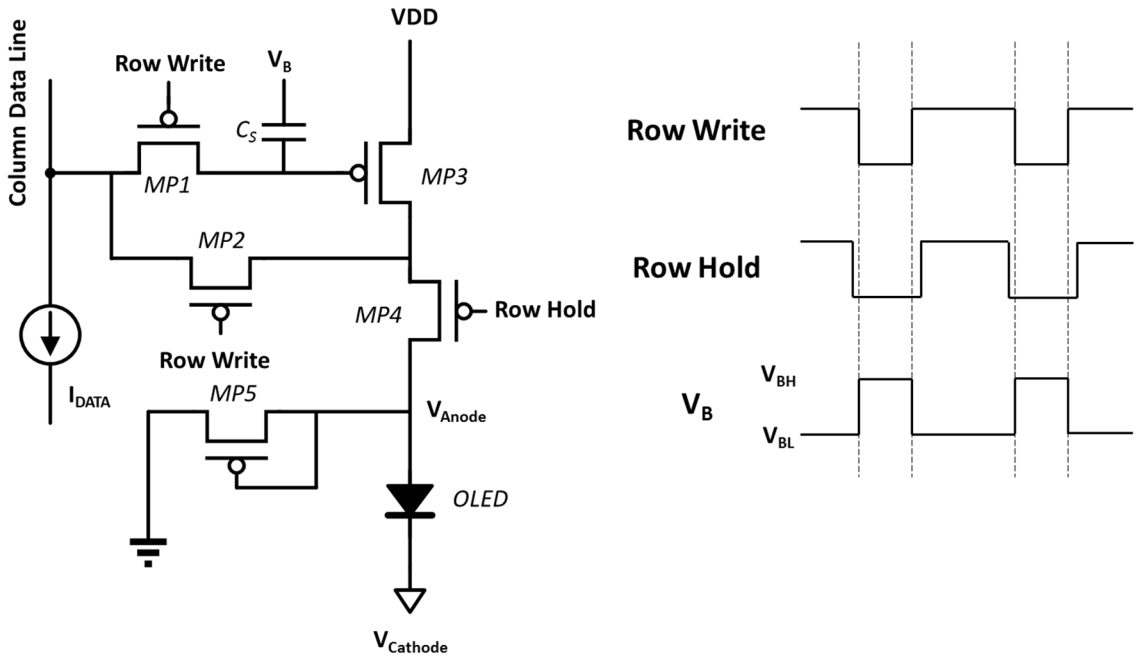


Figure 3-3 Current copier pixel circuit schematic and timing diagram

Figure 3-4 shows a voltage programmed current driving circuit. In this mode, it is possible to achieve a voltage dynamic range from ~0 (ground) to VDD for the OLED, and with a much faster programming time than the current programmed driver. Ideally, the drive MOSFET MP2 is in the saturation region. However, due to the small-scale current of each subpixel, it is more likely that MP2 is biased in the subthreshold or linear region.

In order to find out which operation region is the PMOS in, simulations are performed to compare constant voltage driving pixel (Figure 3-2) and voltage programmed driving pixel (Figure 3-4). Assumed for a 10μm pixel pitch (5μm sub-pixel pitch), the NMOS drive transistor size is chosen to be as large as possible with a W/L=3μm/2μm, and the PMOS drive transistor is specified to be W/L=1μm/3μm. A long PMOS transistor is chosen to reduce its gain. Figure 3-5 shows the simulated OLED current and the derivation of I_{OLED} and V_{DATA} with sweeping V_{DATA}. The dynamic range of constant voltage driver shown is less than the current driving pixel. However, due to the gain of the PMOS transistor and the small sub-pixel current, the current driving pixel is quite sensitive to the change of V_{DATA}. The OLED current is saturated for $V < 3.65V$ and ~ 0 for $V > 4.2V$. Only the voltage range between 3.65V and 4.2V is aplicable to program an appropriate OLED current. On the other hand, for constant voltage driver, the I-V response is a voltage sweep on the OLED with one V_{TH} drop over the drive MOSFET. The constant voltage driving pixel shows better linearity.

Thus, for the voltage programmed current driving pixel, as the current flows to the OLED is highly sensitive to the voltage stored on the capacitor C_S, and leakage could induce sizeable error. Besides, any V_{TH} and mobility variation could seriously affect the pixel-to-pixel luminance uniformity.

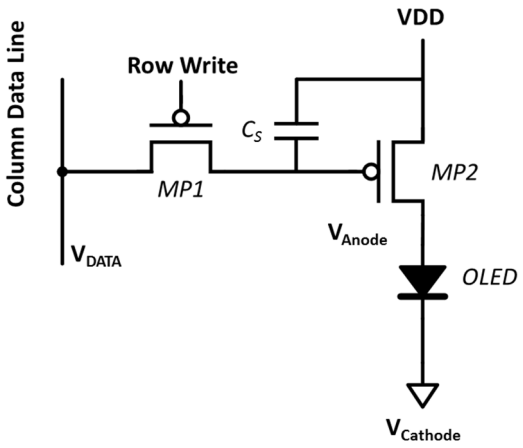


Figure 3-4 Voltage programmed current driving pixel circuit

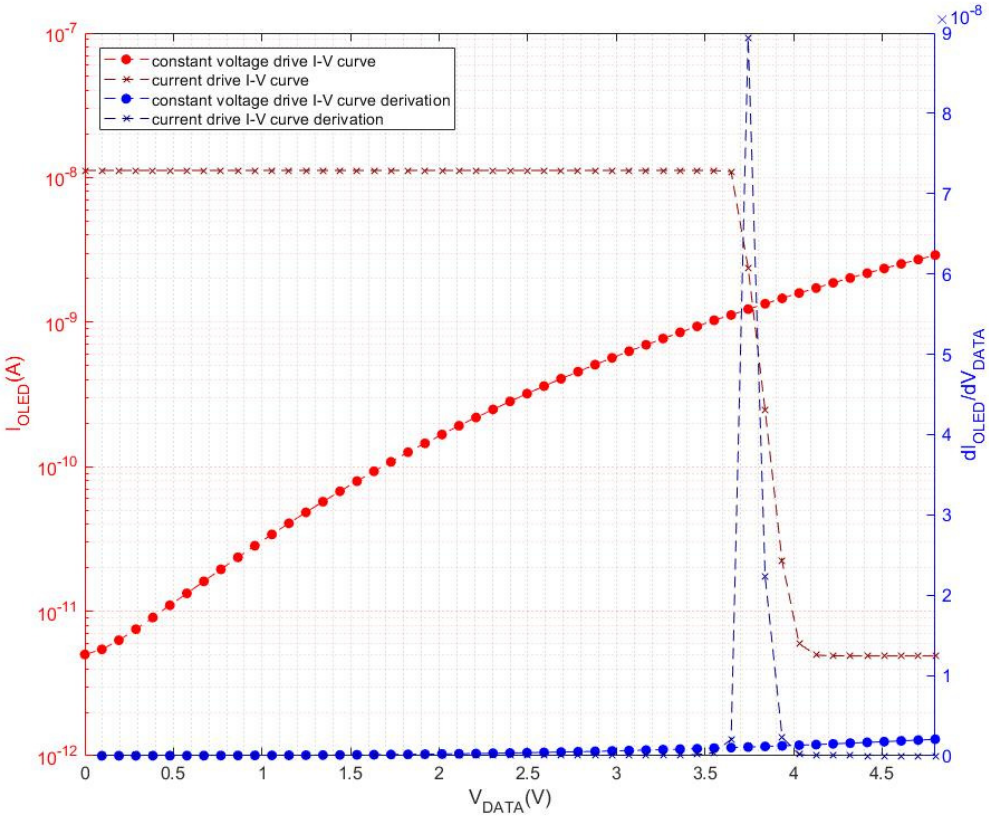


Figure 3-5 Simulation of the constant voltage driving pixel and voltage programmed current driving pixel with sweep V_{DATA} (left y-axis), and their derivatives (right y-axis)

Table 3-2 shows a general comparison of the different types of analogue pixel circuit pros and cons reviewed previously. In these early designs, voltage driving pixel is not popular for its susceptibilities to OLED voltage shift degradation (also known as delta V effect) [149, 150]. However, thanks to the improvement of OLED lifetime [26, 151], there is more voltage driver that published recently. With

few MOSFETs available in the pixel, most microdisplays are in favoured of analogue pixels. However, it is difficult to shrink the pixel size further, as analogue pixels which employed high voltage transistors, do not scale down with CMOS process nodes as digital circuits. The other downsides of analogue pixels are the complexity of the analogue signal processing of the video interface and the analogue signal driver (noise, crosstalk, and mismatch etc.). Besides, a number of threshold voltage compensation scheme pixels have also been demonstrated with better luminance uniformity [26, 45]. However, they usually require more complex timing control which creates difficulties for the design of the peripheral drivers.

Table 3-2 Analogue driving method comparison (more + is better)

	Constant voltage driving [26]	Current programmed current driving [30]	Voltage programmed current driving [148]
Driving MOSFET operation	Saturation	Subthreshold	Subthreshold, linear
Input signal	Voltage	Current	Voltage
Lifetime[20]	+	+++	+++
Luminance Uniformity	++	+++	+
Contrast Ratio	++	+	+++
Leakage induced Flicker	+++	+	+

b) Digital PWM Pixel Circuits

A wholly-digital pixel applies a digital pulse width modulation signal, either a voltage or a current, to the OLED. It is widely used for LCoS [152] and DLP DMD [11, 13] microdisplays, as they are inherently driven by digital pulses. The digital time domain modulation gives a root mean square voltage/current level for generating grayscale, as shown in Figure 3-7 (a). The observer's eye will interpret the ON/OFF digital pulses as analogue brightness levels [153]. The pulses must be fast/frequent enough to accommodate the grayscale, prevent perceivable flicker.

[20] Change of luminance as OLED ages

Figure 3-6 shows a historical example of a digital pixel circuit [18]. An 1-bit SRAM storage is implemented each pixel. The 1-bit SRAM controls the on/off of PMOS switch Q5. The current is generated by the current source Q3. As the pixel current is tiny, the Q3 is designed to be a long MOSFET (W/L=2.64μm/79.12μm) to operate in the saturation region. Besides, the relatively large channel Q3 minimizes the pixel-to-pixel variation. The power consumption for data refreshing is low, as only the pixels, which have a change in luminance, need to be updated. The raster-scan row/column driver design is also more straightforward than the analogue pixels. The pixel data can be addressed without any display controller. However, it requires a high clock rate and high data transfer. Depending on how many bits of SRAM and DRAM stored in-pixel, the digital pixels demand large pixel pitch. The pixel pitch of the example pixel is 34.3μm, and the total display is eventually 1.08 inch diagonal. Nevertheless, the digital pixel benefits significantly from the size shrink of the logic gates for small pixel pitch. Voltage level shifter is required for the reduced V_{DD}. Underwood et al. have implemented a 12 μm sub-pixel pitch with 6-bit DRAM in-pixel which are switching the OLED ON/OFF sequentially [31, 154].

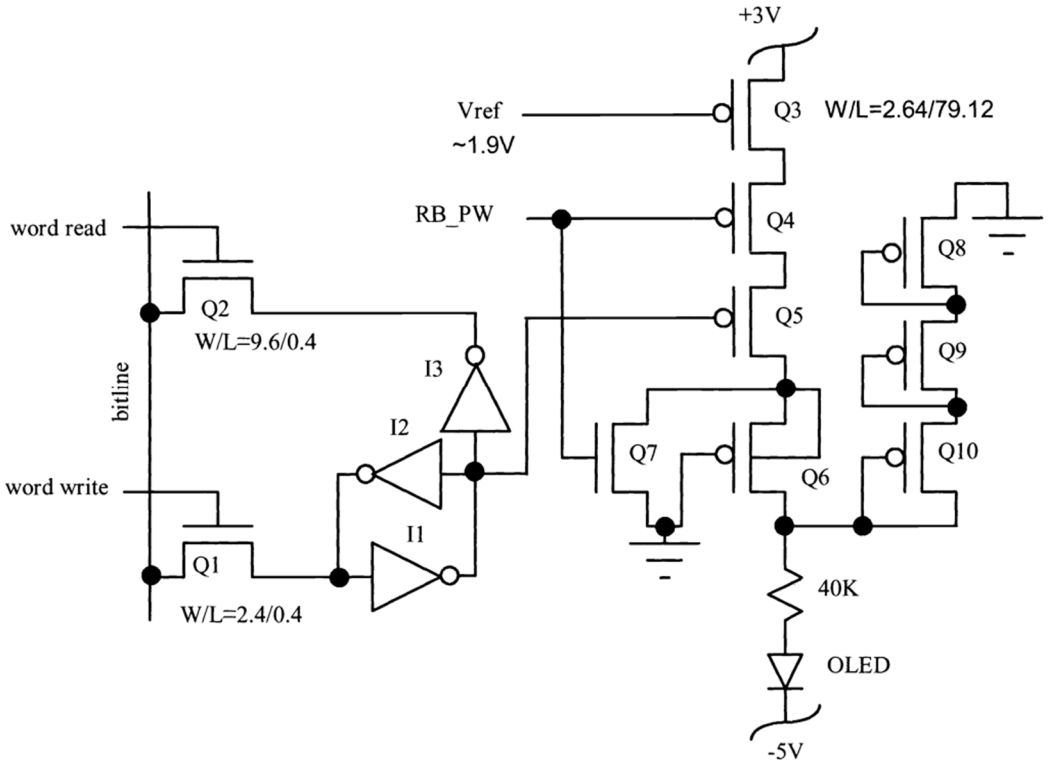


Figure 3-6 Example digital pixel schematic (source [18])

c) Analogue PWM Pixel Circuits

The analogue PWM approach gives an alternative option to analogue and digital PWM pixels. In analogue PWM pixels, an analogue input signal is sampled and held for each frame. The pixel driver is in principle an analogue to time converter (ATC) – convert an analogue signal to a time pulse width.

The grayscale is created by the pulse width, as shown in Figure 3-7 (c). A single pulse is usually created by comparing the in-pixel stored signal with a global ramp signal [154]. The ramp signal can be reshaped to realise gamma correction without compensating the input DATA signal [155]. The frame update technique is similar to the analogue drivers. Instead of sequentially updating of all the SRAM/DRAM cells for a digital pixel, the analogue pixel only needs to update once every frame. The analogue PWM pixel also allows a high dynamic range pulse width output. However, the in-pixel comparator increases the transistor count (>10T), resulting in a relatively large pixel. Besides, the static bias current for the analogue comparator increases the pixel static power consumption. It also suffers luminance non-uniformity caused by the analogue effects (e.g. mismatches) like the other analogue pixels.

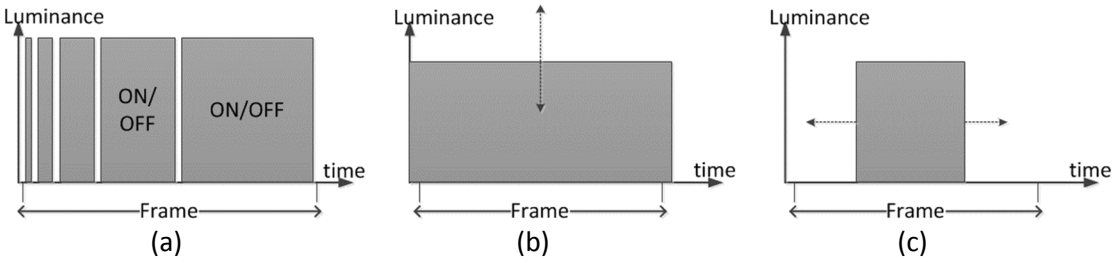


Figure 3-7 Greyscale generation from (a) digital pixel, (b) analogue pixel and (c) analogue PWM pixel.

3.4.2 Advanced pixel circuit design

The main difference between driving a TOLED and a conventional OLED is the high built-in voltage and the wide voltage range to control the current. Thus, it demands a high voltage and high voltage dynamic range driver. Apart from the pixel circuits that have been shown in the previous section, there are a number of novel pixel driver published recently. We will discuss some of them that have the potential for driving TOLEDs.

3.4.2.1 High dynamic range constant voltage driver

A constant voltage driving pixel with improved dynamic range has been reported by Wacyk et al. [151, 156]. A pixel pitch of 12 µm (4×12 µm^2 sub-pixel) is realized for the design. The pixel schematic is shown in Figure 3-8 (a). It is based on a conventional constant voltage driving pixel as shown in Figure 3-2. The 'Row Write' switch is implemented by a transmission gate MN1 and MP1 to extend the programmable dynamic range V_{DATA}. The pixel uses two extra MOSFETs, MN3 and MP2, to extend the range of low voltage output current. V_{bias2} is set to about one V_{th} below ground, and V_{bias1} is set to about one V_{th} above ground. When V_{DATA} is at a relatively high level, MP2 acts as a closed switch in the linear region of operation (low impedance). When V_{DATA} is at a low level (low luminance levels), the source terminal of MN2 V_S approaches zero. Thus, MP2 enters the subthreshold region. The current flow to the OLED is exponentially dependent on $V_{GS\_MN2}=V_S-V_{bias2}$. As V_{DATA} drops, the output current of MP2 reduces rapidly and cuts off the OLED. The MN5 acts a load for the current flow from MN2 when V_{DATA} is at a low level.

As shown in the simulation in Figure 3-8 (b), the standard voltage drive (similar to Figure 3-2) has a limited dynamic range when $V_{DATA} \leq V_{TH}$, where the drive transistor is biased in subthreshold. For this pixel driver, the response is similar at high V_{DATA} levels. However, the low voltage improvement can drive the OLED nearly two orders lower compared to the conventional driver. A contrast of greater than 10,000:1 is reported with the new pixel design.

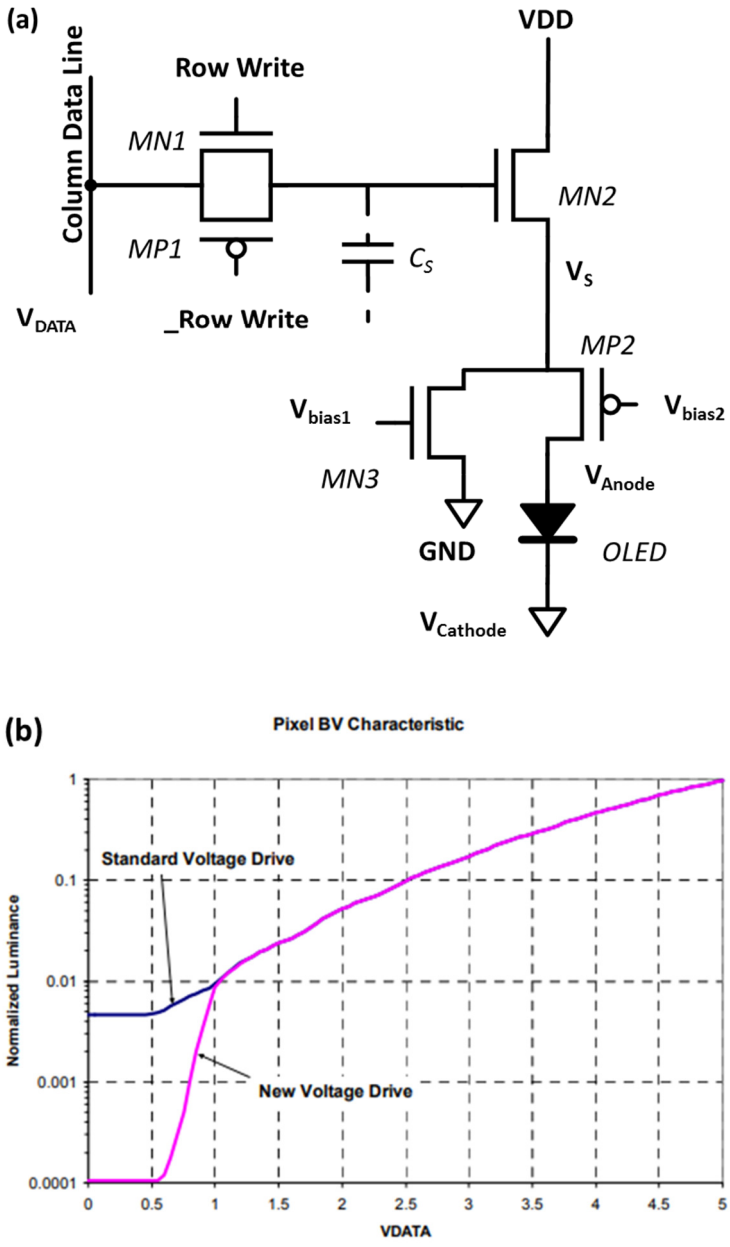


Figure 3-8 (a) improved voltage dynamic range constant voltage driving pixel (b) simulated voltage drive response (source [151, 156])

3.4.2.2 V_T compensation constant voltage driving pixel

Apart from the lack of dynamic range mentioned above, another deficiency for the constant voltage driver is the V_{TH} and mobility variations. There are some published pixel circuits that can perform V_{TH} and mobility compensation [45, 157-159]. However, they usually require extra in-pixel transistors and control signals which is hard to implement in Microdisplay with a small pixel pitch. Onoyama et al. reported a compensation pixel circuit that consist of only two NMOS and two capacitors, as shown in Figure 3-9 (a). MN1 is the switch for programming voltage, and MN2 is source follower driver for the OLED. C_1 stores the driving voltage for MN2 over a frame time, which could be a MiM (metal insulator metal) capacitor or the gate-source capacitance of MN2. C_2 can be the parasitic capacitance of the OLED device. The timing diagram is shown in Figure 3-9 (b). At the reset stage, DS is switched from VDD to V_{ini} to reset the OLED device. Later, at the V_{th} cancel stage, MN1 is switched on, V_{ofs} (offset voltage in Figure 3-9 (b)) is sampled to the gate of MN2. The V_{ofs} is set to about one V_{th} above ground. When DS changes to VDD, the OLED anode voltage is V_{ofs}-V_{th} as the OLED current is tiny. The voltage stored on C_1 is V_{th}. Then in the data writing stage, V_{signal} (signal voltage) is sampled to the gate of MN2. The OLED starts to charge up. MN1 is switched on for a determined amount of time. V_{anode} is charged up by ΔV_S. The gate-source voltage of MN2 becomes V_{signal}-(V_{ofs}-V_{th})-ΔV_S. The current flow to the OLED is,

$$\begin{aligned} I_{OLED} &= \frac{1}{2}\frac{W}{L}\mu C_{ox}(V_{GS} - V_{TH})^2 \\ &= \frac{1}{2}\frac{W}{L}\mu C_{ox}\left(V_{signal} - V_{ofs} + V_{TH} - \Delta V_S - V_{TH}\right)^2 \\ &= \frac{1}{2}\frac{W}{L}\mu C_{ox}\left(V_{signal} - V_{ofs} - \Delta V_S\right)^2 \end{aligned}$$

Equation 3-1

Therefore, V_{th} is cancelled out, and ΔV_S can compensate the mobility mismatch. A sub-pixel pitch of 3.3×9.9μm is achieved with in-pixel uniformity compensation.

However, there are two assumptions which the compensation scheme is based on, could be unfeasible in reality. The V_{TH} of MN2 suffers from body effect. The value is changed with V_{anode}. The assumption that V_{TH} of V_{DATA}=V_{signal} and V_{DATA}=V_{ofs} can be cancelled out could be wrong. Besides, the mobility compensation may be not practical. A row of pixels shares the same "Row Write" signal. It is difficult to control an individual MN1 on time to generate a specific ΔV_S for the pixels that are in the same row.

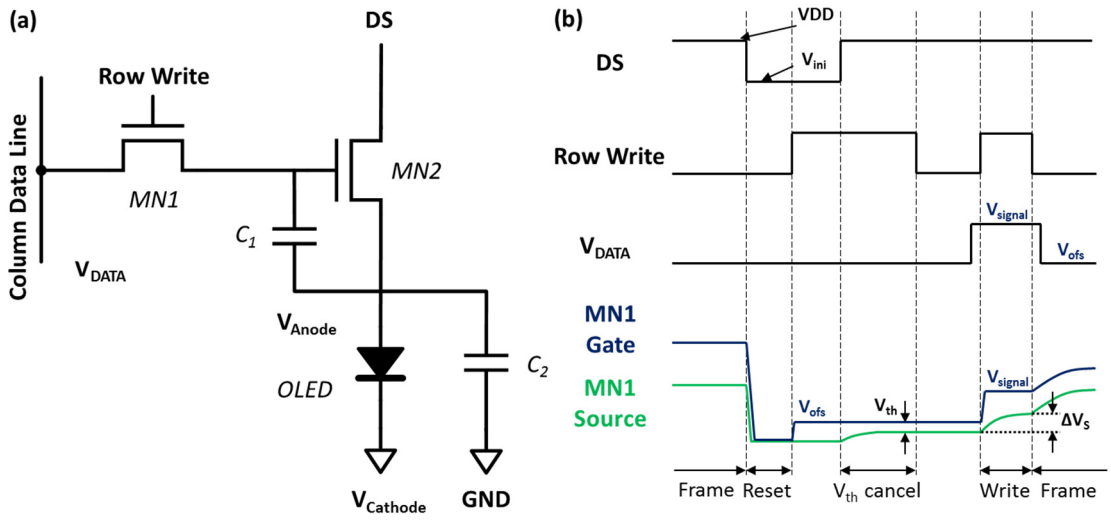


Figure 3-9 (a) V_{th} compensation constant voltage pixel driving circuit (b) timing diagram

3.4.2.3 Digital PWM pixel

Instead of the analogue pixels mentioned previously, there are OLED microdisplays that employ a digital driving approach with improved performance. Figure 3-10 shows a digital pixel proposed by Vogel et al. [160] The pixel composed both 1.8V transistors and 5V transistors. There are 8-bit of DRAM and read/write circuits that consist of 1.8V transistors. The output of DRAM cells is connected to the sense amplifier. It acts as a level shifter to control the high voltage switches M_{Swi} and M_{NSwi}. Constant voltage V_{Drive} is applied to M_{Drive} to supply a constant current to the OLED when it is switched on. The 8-bit DRAM is selected sequentially to produce a PWM output.

The use of low voltage DRAM cells which scale with CMOS process node is helpful to the miniaturisation of the pixel area. However, the voltage difference between on- and off-state of an OLED is high. 5V/3V transistors are required for output. Thus, both the sense amplifier (level shifter), the current driver, and the switches (M_{Drive}, $M_{Goff,}$ and M_{Swi}) are high voltage transistors. In this design, a pixel pitch of 16µm, sub-pixel pitch 8µm (RGBW structure) is achieved. If a more advanced CMOS process is employed, the DRAM cells can be replaced by SRAM cells (reliable, low power but with more MOSFETs). It is possible to further reduce the pixel size. However, care must be taken for the leakage current, decreased breakdown voltage.

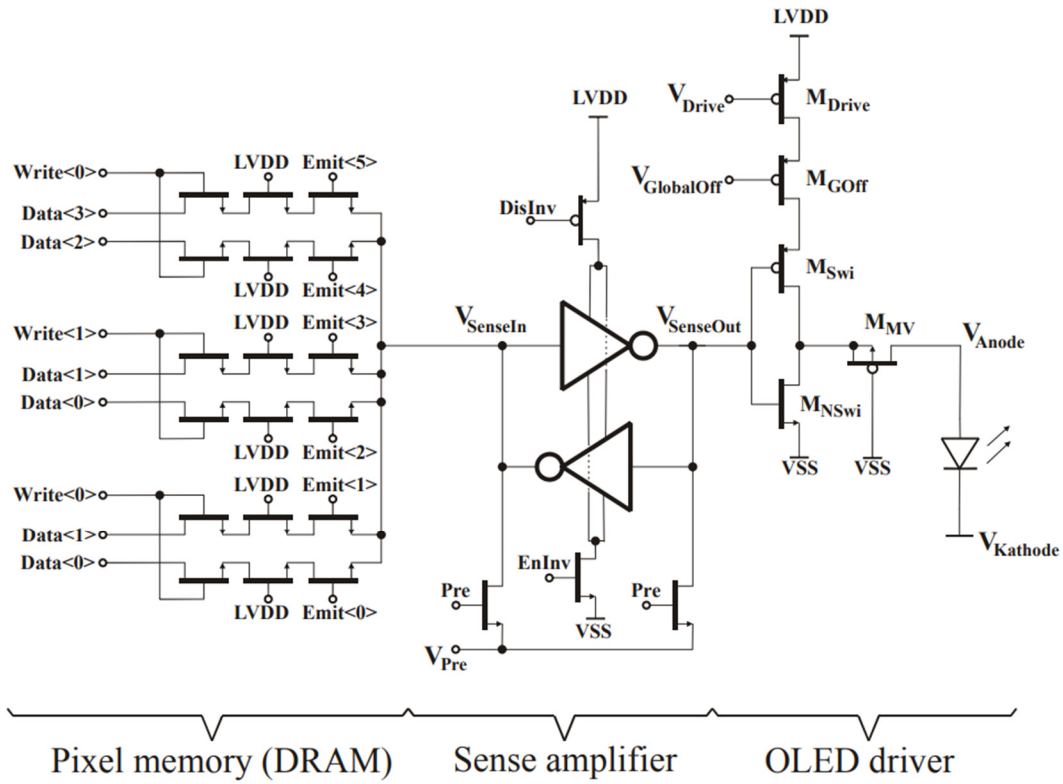


Figure 3-10 Schematic of a digital pixel with in-pixel low voltage DRAM cells (source [160])

3.4.2.4 Analogue PWM pixel

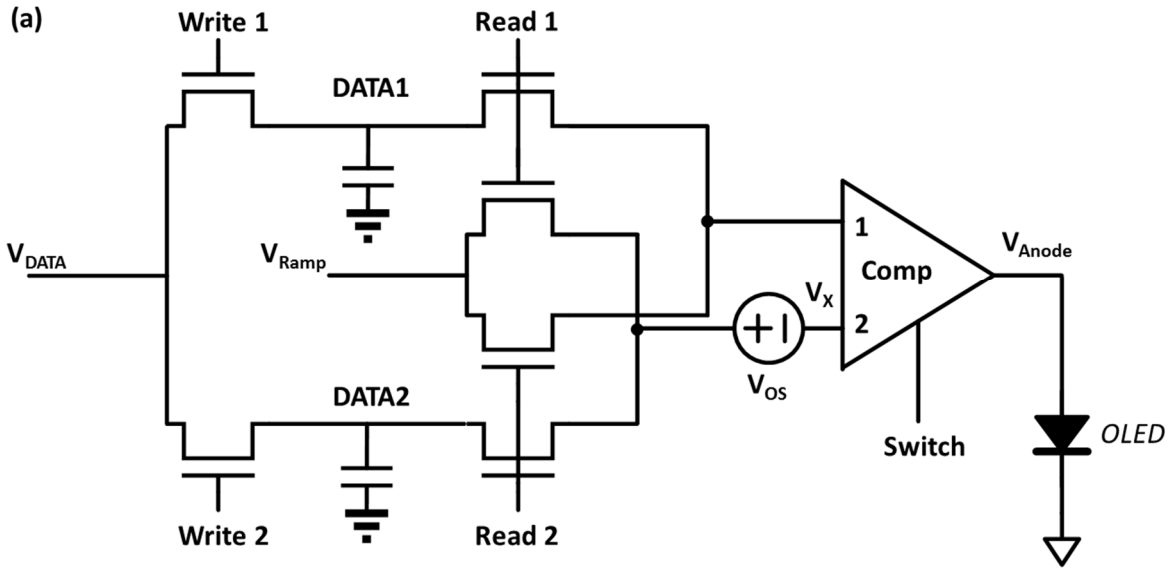
Analogue PWM pixel is not a very popular choice for OLED microdisplays. One of the reason could be the design complexity. It is a challenge to design an analogue to time converter in-pixel to generate a pulse width. The design and transistor sizing are critical to realize a small pixel pitch without severe impairment to the pixel function.

Blalock et al. presented an analogue PWM based pixel driver with offset correction [6]. The pixel was initially applied for FLC microdisplays. Afterwards, Abraham et al. reported the use of the backplane for a polymer OLED microdisplay [20].

The pixel circuit schematic is shown in Figure 3-11 (a). The column V_{DATA} is sampled and held by the Write 1 (or Write 2) switches. V_{Ramp} is a rising ramp voltage which reset every half display period. When Read 1(or Read 2) is asserted, the comparator inputs are connected to DATA1 (or DATA2) and V_{Ramp}. The two-stage differential PMOS input comparator composes 11 transistors. By asserting/de-asserting the Switch signal, the output stage is connected to either of the input differential pair outputs. It switches the positive and negative terminal of comparator between input 1 and input 2. The comparator offset voltage is modelled as V_{OS}.

Figure 3-11 (b) shows the timing diagram of the circuit operation. Within each display cycle, the Switch signal is set on/off symmetrically half a display cycle. On the first display cycle, V_{OS} is in series with DATA2 signal presented to the comparator. The Switch signal is high for the first half display cycle. The comparator positive terminal connects to V_{Ramp}, and the negative terminal connects to $V_X=V_{DATA2}-V_{OS}$. The V_{Anode} signal is switched on early for a proportion of V_{OS}/V_{DATA2}. On the second half of the same display cycle, Switch signal is set low, the positive and negative terminal of the comparator exchanged. The negative terminal connects to V_{Ramp}, and the positive terminal connects to V_X. The V_{Anode} signal is switched from high to low earlier for the same amount of time (V_{OS}/V_{DATA2}). The V_{OS} error is compensated with the total pulse shifted to the left. On the next display cycle, V_{OS} is switched to be in series of V_{Ramp}. The V_{Anode} pulse is shifted right with V_{OS} compensated by the Switch signal.

The Blalock pixel proposed a way to compensate the comparator offset voltage that is introduced by the mismatch. The resulting standard deviation of the variation of single pulse width is 2.3%. Gamma correction is allowed by incorporating a reshaped V_{Ramp}. High dynamic range is realized (>8 bit[21] [31, 161]), depends on the column driver DAC. The frame rate can be as high as 225Hz. However, the high number of analogue transistors (17T2C) led to a relatively large pixel pitch – 12μm, monochrome. It is difficult to shrink the pixel unless the comparator can be designed differently. Also, the comparator bias currents consume extra static power.



[21] The state of the art publication is 6-bit

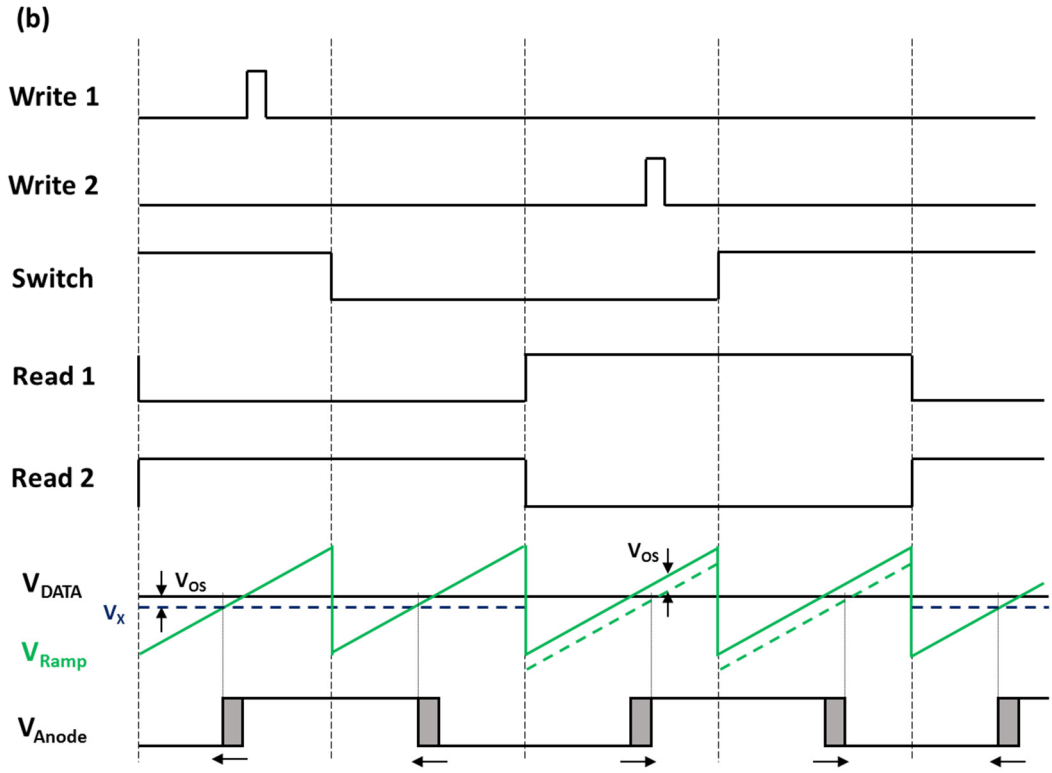


Figure 3-11 (a) Analogue pulse width modulation pixel circuit (source [6, 20]) (b) timing diagram

3.5 Pixel circuit design and simulation

This section details the design, implementation and characterisation of test pixel arrays to prove the concept that an analogue in-pixel pulse width modulation pixel can be designed to be scalable in pixel pitch combining their inherent advantage high dynamic range and gamma correction. We have designed and tested one improved performance constant voltage driving pixel and three different analogue PWM pixel arrays with a state of the art sub-pixel pitch of 4.7, 5, and 5.05µm.

A photomicrograph of the test arrays is shown in Figure 3-12. The test arrays have been fabricated in STMicroelectronics' 130nm Microdisplay CMOS process[22] (1 poly and 5 metal, P+ substrate). The thick oxide transistors operating voltage is 4.8V, and 1.2V for thin oxide transistors. These arrays have been deposited with white tandem structure OLED stacks provided by CEA Leti/MicroOLED through the ENIAC POLIS project.

The simulations presented in this chapter are performed in Cadence with CMOS device model supplied by STMicroelectronics for HCMOS9A process, and the tandem OLED model presented in section 2.7.

[22] STMicroelectronics HCMOS9A LED/DISPLAY130
https://www.st.com/content/st_com/en/about/innovation---technology/BiCMOS.html

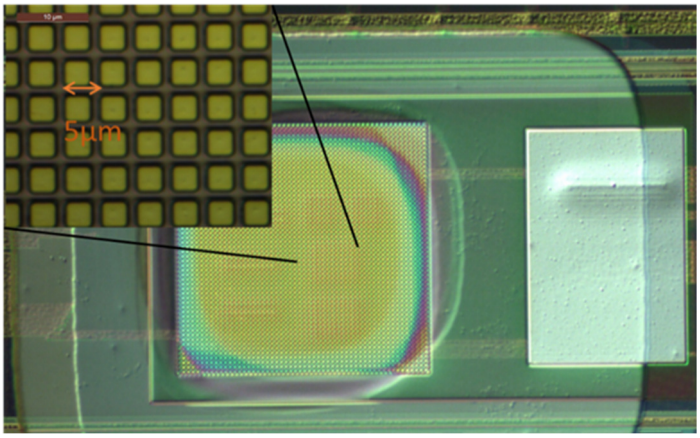


Figure 3-12 Photomicrograph of the test array. The zoom inset shows the layout of the pixel test array

3.5.1 Sample and Hold

For analogue pixel drivers with an analogue signal input (either current or voltage), a compact sample and hold stage is critical for maintaining the signal for a display frame to reduce flicker. The sample and hold stage usually consists of a switch and a memory storage capacitor. For example, the two constant voltage driving pixel as in Figure 3-13, the NMOS transistor switch and the capacitor in the blue box is the sample and hold elements. A voltage V_{DATA} is written to the capacitor C_S at the start of a display frame. The voltage is then held until the end of the frame.

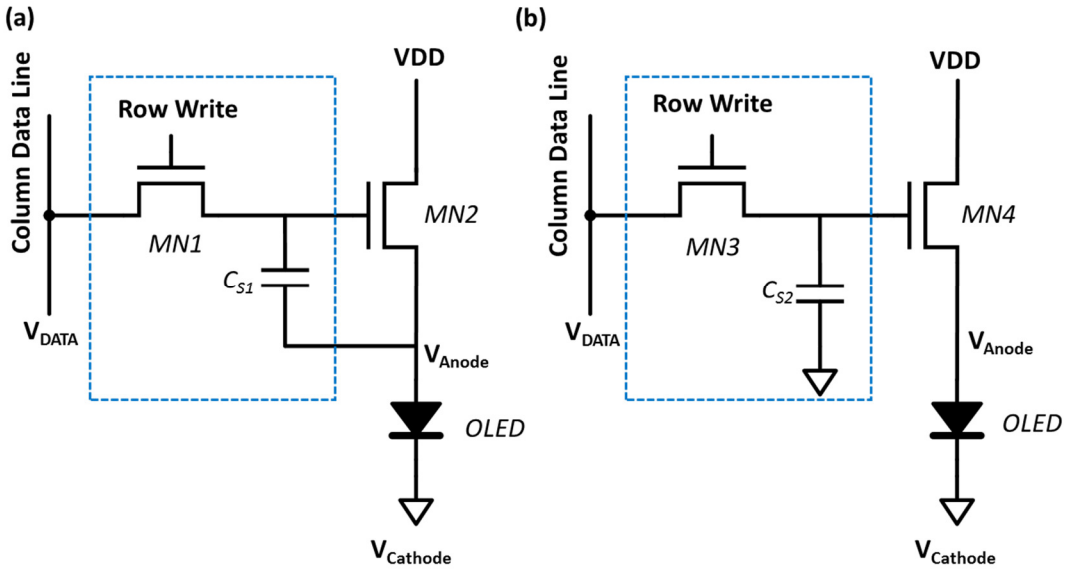


Figure 3-13 Sample and hold stage for constant voltage driving pixel

3.5.1.1 MOS capacitor

There are several types of capacitor available in the CMOS processes, including MIM (metal-insulator-metal), MOM (metal-oxide-metal), as well as MOS (metal/poly-oxide-semiconductor). Due to the

constraint of the selected CMOS process[23], MIM capacitors are not considered. The MOM capacitance varies between 0.66 and 1.32 fF/μm^2, depending on the finger length and the number of fingers. One way to implement MOS capacitor is N^+ poly-oxide-N-well (similar to a PMOS), the benefit is an independent voltage can be applied to both terminals of the MOS capacitor (positive terminal connected to N-well and negative terminal connected to N+ poly), and a relatively constant capacitance (3.7fF/μm^2). However, the layout of the N-well spacing consumes extra area. The other option for the MOS capacitor is to implement an NMOS cap which offers a higher capacitance than the MOM capacitors. The limitation of the NMOS cap is that the capacitance value would vary with the bias voltage, and one of the terminals needs to be connected to ground. To extract the capacitance in a sample and hold circuit as shown in Figure 3-13, we assumed that the capacitor C_{S1} is the gate-source capacitance of MN2 (W=3μm, L=2μm), C_{S2} is a MOS cap (W=2μm, L=2μm), MN1/MN3 are minimum transistor (W=0.5μm, L=0.5μm) and MN4 is W=1μm, L=1μm. The simulated capacitance with sweeping V_{DATA} is shown in Figure 3-14. The MOS cap in the inversion region ($V_{GS}>V_{TH}$=0.6V), the depletion width and the capacitance reaches a maximum value. For $0<V_{GS}<V_{TH}$, the MOS cap is in the surface depletion region, the depletion width varies with a bias voltage. The extracted capacitance is consistent with the empirical model [162].

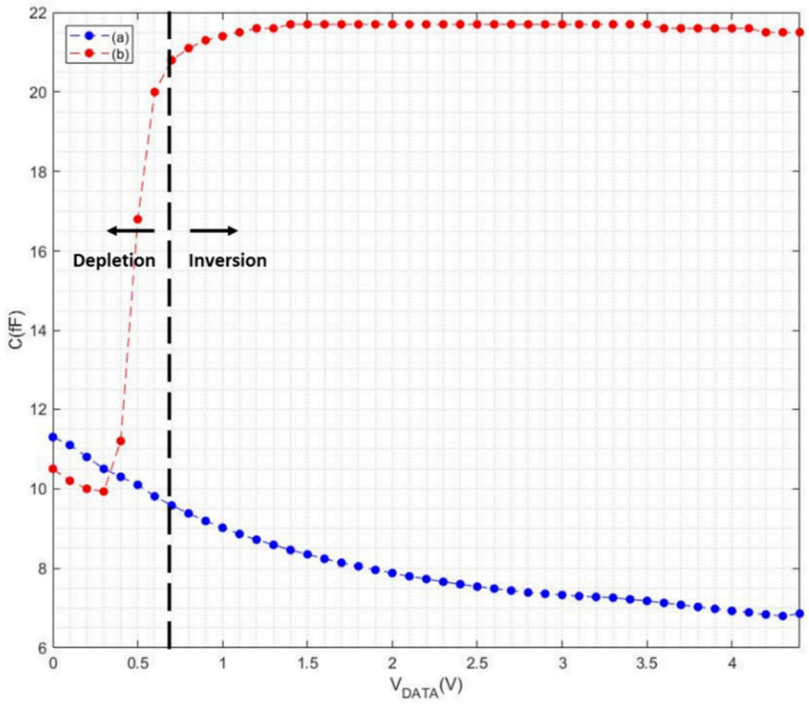


Figure 3-14 simulated capacitance of the sample and hold circuits shown in Figure 3-13(a) and (b)

[23] For HCMOS9A LED, the MIM capacitor is implemented between the top metal layer (metal 4) and the ALUCAP, the electrode terminals need to be connected to an ALUCAP plate which is contacting the OLED material deposited on top.

3.5.1.2 In-pixel stored analogue voltage leakage flicker

In order to explore the leakage effect on the current flow through the OLED, the conventional 2T constant voltage driving pixel in Figure 3-13 (a) is employed for simulations. Figure 3-15 illustrates the timing diagram and the flicker effect. When MN1 turns on, V_C is charged to V_{DATA}. When the Write signal turns off, there is a small voltage drop caused by charge injection and clock feedthrough. Then, during the emission time of a frame, leakage from the storage node causes OLED current flicker. During this process, there are a few behaviours that are needed to be analysed. First, it should have enough ON time for the Write signal. So V_C could charge up to a level close to V_{DATA}. Second, it is essential to know how much the charge injection is. Third, the current flicker should be reduced to an acceptable level that there is no visible change in brightness.

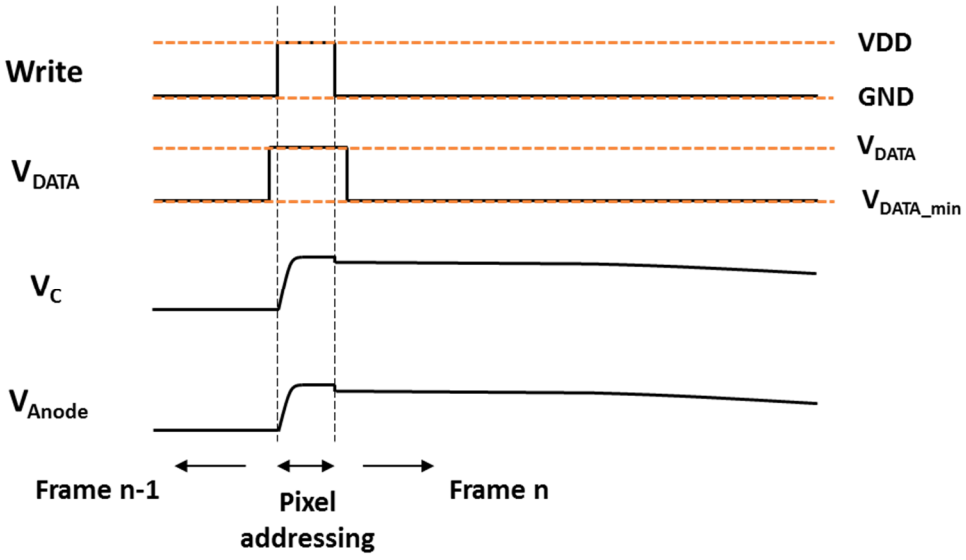


Figure 3-15 2T voltage driving pixel timing diagram and flicker effect

The time of charging up the capacitor is about five time-constants $R_{ON}C$. R_{ON} is the ON resistance of the switch. For a V_{DATA} that small enough to avoid cut-off of MN1 (V_{GS}=VDD-V_{DATA}>V_{TH}), the settling time constant $R_{ON}C$ is mostly determined by the R_{ON} of the NMOS switch in the linear region of operation, where V_{DS}=V_{DATA}-V_S<V_{GS}-V_{TH}. R_{ON} can be given as,

$$R_{ON} = \frac{\partial v_{DS}}{\partial i_D} = \frac{L}{\mu_n C_{ox} W (V_{GS} - V_{TH})} \qquad \textbf{Equation 3-2}$$

Where μ_n is the mobility of electron and C_{ox} is the capacitance of the oxide layer. R_{ON} is inverse proportional to V_{GS}-V_{TH}, the higher the V_{DATA}, the longer the settling time is. Figure 3-16 shows the simulation of settling time versus V_{DATA}. The settling time is the time interval between the switch turn-on and the V_C charged 0.01% error of V_{DATA}. As V_{GS} approaches V_{TH}, the switch starts to turn off. For V_{DATA} higher than 3.9V, there is no settling of V_C within 0.01% error in less than 10ms, which indicates

the V_{TH} increased due to the body effect. For V_{DATA}≤3.8V, the settling time is less than 1μs. In this simulation, the output impedance of the column DATA driver is ignored here by assuming the R_{ON} is dominant in comparison.

When the Write signal turns off, both clock feedthrough and channel charge injection from parasitic of MN1 are coupled to C_{S1}. The stored voltage suffers a small voltage drop. There are some methods to cancel the charge injection, e.g. dummy switch, complementary switch [163]. However, additional transistors are required in these cases. Implementation within the required pixel pitch is difficult. Thus, it is worth to know the level of charge injection and compensate with lookup table correction. The charge injection[24] can be approximated by,

$$\Delta V_{Charge\ injection} = \frac{Q_{ch}}{2C_{S1}} = \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{2C_{S1}}$$

$$V_{out} = V_{in} - \Delta V = V_{in}\left(1 + \frac{WLC_{ox}}{2C_{S1}}\right) - \frac{WLC_{ox}}{2C_{S1}}(V_{DD} - V_{TH}) \quad \textbf{Equation 3-3}$$

If the clock feedthrough is included, the equation becomes,

$$\Delta V_{clock\ feedthrough} = V_{DD}\frac{WC_{ov}}{WC_{ov} + C_{S1}}$$

$$V_{out} = V_{in} - \Delta V = V_{in}\left(1 + \frac{WLC_{ox}}{2C_{S1}}\right) - \frac{WLC_{ox}}{2C_{S1}}(V_{DD} - V_{TH}) - V_{DD}\frac{WC_{ov}}{WC_{ov} + C_{S1}} \quad \textbf{Equation 3-4}$$

where C_{ov} is the overlap capacitance per width, C_{S1} is the storage capacitor in Figure 3-13 (a) and W/L is the width/length of transistor MN1. The coefficient of V_{in} (V_{DATA}) becomes $\left(1 + \frac{WLC_{ox}}{2C_{S1}}\right)$. Figure 3-17 shows the simulated voltage drop induced by charge injection and clock feedthrough versus different levels of input V_{DATA}. The voltage drop is not linearly decreasing according to V_{DATA} as in Equation 3-4. The reason could be the dependence of the capacitance C_{S1}, which decreases with V_{DATA}. Besides, another possible reason is the falling time of the Write signal [164-166]. If the falling rate is slow, most channel charges is return to the source (V_{DATA}) which reduce the charge injection. The falling time is assumed to be 100ps in the simulation, it could be different in reality.

After that, during the emission of a frame, only the off switch leakage current could affect the stored voltage and the OLED current. The luminance flicker level is dependent on the level of leakage current. The leakage current in the off state, for the long channel and thick oxide device[25], is dominated by the

[24] Assume half of channel charges is injected to C_{S1}
[25] Drain induced-barrier lowering and gate oxide leakage effects are negligible.

MOSFET subthreshold current. For $V_{TH}>V_{GS}>V_{FB}$ (flat-band voltage), some minority carrier electrons can overcome the energy barrier and diffuse from source to drain. The subthreshold current is small, but become significant when V_{GS} is close to V_{TH}. If the gate voltage further reduces to $V_{GS}<V_{FB}$, the majority carrier holes start to accumulate under the gate region. The conduction of minority carrier electrons between drain and source are cut-off by the accumulating p-type carriers under the gate. Flat-band voltage is the electrostatic potential difference between the P-substrate work function ϕ_P and gate metal work function ϕ_M. It is usually negative,

$$V_{FB} = \phi_P - \phi_M \qquad \textbf{Equation 3-5}$$

After a pixel has been addressed, the Write signal is set to ground. The gate-source voltage becomes,

$$V_{GS}(OFF) = V_{Write} - V_{DATA}(Next) = -V_{DATA}(next) \qquad \textbf{Equation 3-6}$$

where V_{DATA} (next) is the DATA voltage for the pixel on the next rows. If $-V_{DATA}$ (next) $\leq V_{FB}$, the MOSFET subthreshold leakage current is negligible. The worst case flicker happens when only one pixel in a column is emitting; other pixels are addressed to the minimum level of V_{DATA}. Thus, if the minimum V_{DATA} is higher than $|V_{FB}|$, the flicker would be minimised. Figure 3-18 shows the worst case leakage simulation performed for the 2T constant voltage driving pixel. The OLED current flicker percentage in 10ms with a 2.5V V_{DATA} stored in pixel (2.3V with charge injection). V_{DATA} is set to the minimum level after addressed. The current flicker level is up to ~70% for V_{DATA} (min)=0 and reduces to less than 5% for minimum $V_{DATA}\geq$80mV.

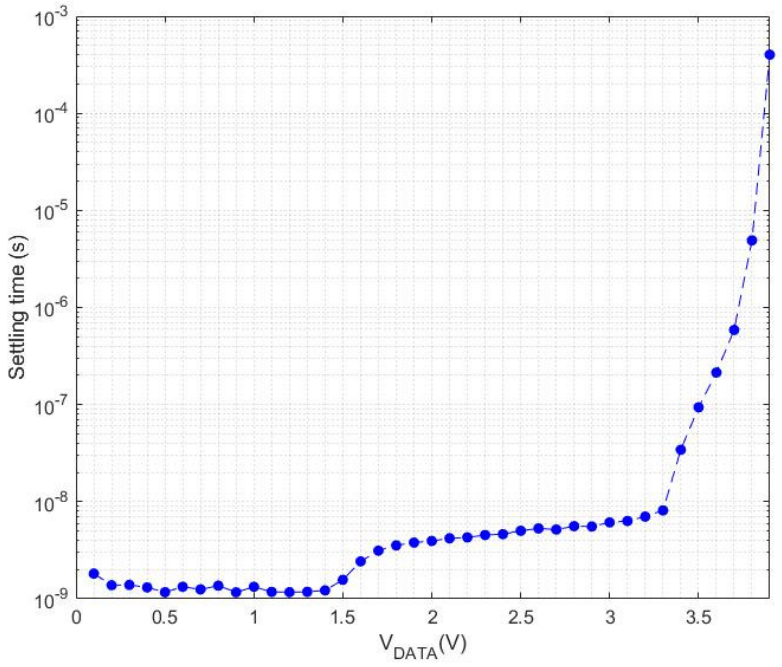


Figure 3-16 2T voltage driving pixel 0.1% settling time with sweeping V_{DATA}

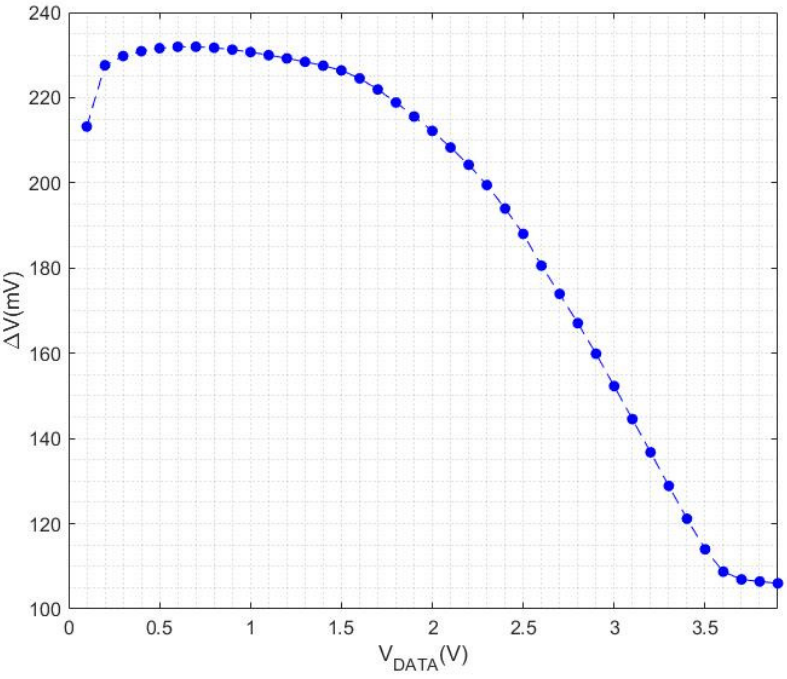


Figure 3-17 charge injection and clock feedthrough voltage drop versus V_{DATA}

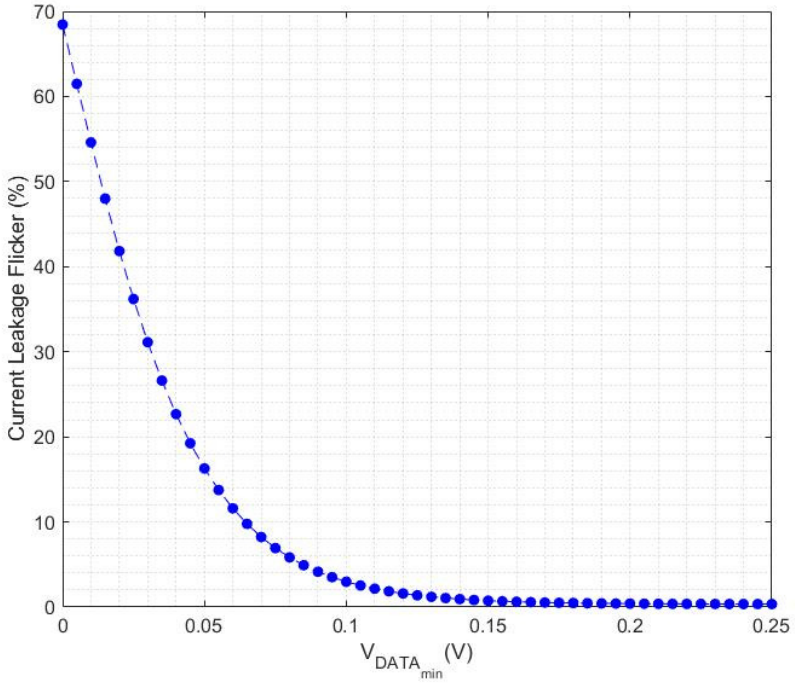


Figure 3-18 worst case leakage simulation, current flicker level versus the minimum level of V_{DATA}

3.5.1.3 Annular transistor

The dynamic range of the SF pixel is lowered for the need of increasing the minimum V_{DATA} to reduce pixel leakage. It is worth to explore other methods to reduce the leakage of the sample and hold circuit. Thus, we implement a variation of the 2T SF pixel with an annular transistor as the switch MN1 in Figure 3-19 (b). The conventional transistor layout is shown in Figure 3-19 (a). Their edges are known to be susceptible to radiation-induced leakage [167, 168]. The "edgeless" annular transistors are employed in radiation hardened environment, e.g. aerospace, military environment. OLED microdisplays are usually not exposed to radiation environments. However, the light emitted from the organic layers can penetrate to the substrate through the gaps between pixel metal plates, causing photo-currents.

For annular transistors, the inner/internal and outer/external terminals are asymmetric with different junction area. The inner terminal (assume source) has a reduced junction area and less depletion capacitance. On the other hand, the external terminal capacitance is higher. Besides, the annular shape of the gate modifies channel electric field. The electric field intensity becomes inversely proportional to the drain area [168]. Thus, the unique structure offers the properties:

- Less charge injection from the inner terminal for reduced capacitance
- The reduced electric field at the outer terminal improved radiation tolerance

However, the downside is that the minimum size the annular transistor can achieve is still much larger than a regular transistor. The annular shape layout, as shown in Figure 3-19 (b), extracts a size of W/L=3.12µm/0.54µm. The pixel size of the 2T SF pixel increases from 4.7µm to 5.05µm. Figure 3-19 (c) and (d) shows the layout of 2×2 2T SF pixel with regular switch and annular switch, respectively. There is no model exists in the CMOS process library for the annular transistor. Simulation and detail analysis of annular transistor would require TCAD tools. The 2T SF pixels with both regular rectilinear MOSFET and annular shape MOSFET are implemented for comparison.

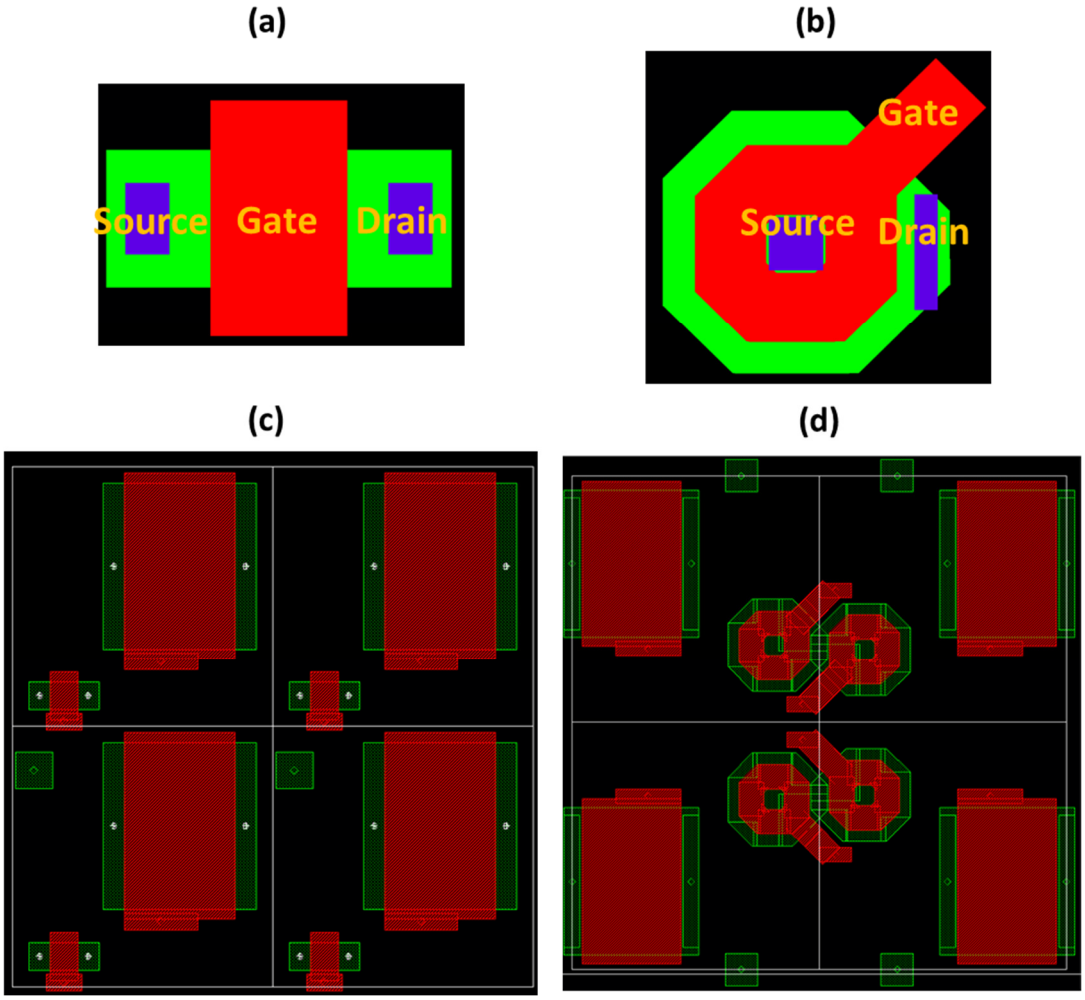


Figure 3-19 (a) Normal switch layout (b) Annular switch layout (c) layout of 2×2 2T SF pixel, 4.7µm sub-pixel pitch (d) layout of 2×2 2T SF pixel with annular switch 5.05µm sub-pixel pitch

3.5.2 Analogue PWM pixel

Section 3.4.2.4 described the architecture of an analogue PWM pixel – in principle, an analogue to time converter. The analogue PWM pixel driver can cover the full voltage dynamic range with a binary output of GND and VDD, which is advantageous for TOLED. Additionally, it retains the benefits of an analogue level input with a lower operating frequency than the digital pixels. The challenge is the scaling of the analogue PWM drivers to fit in a state-of-the-art pixel pitch (~10μm, ~5μm sub-pixel pitch) to allow a high dynamic range output and a reasonable level of uniformity.

3.5.2.1 Operation

The proposed analogue PWM pixel, with a more straightforward analogue to time converter, consists of five MOSFETs and one MOS capacitor. Figure 3-20 presents the schematic diagram of the pixel circuit. The sample and hold stage consists of MOSFET MN1 as a switch and MOSFET MC as a storage MOS capacitor. The column DATA signal is sampled onto the dynamic memory capacitor MC once every frame. The gate and source terminal of MOSFET MN2 is considered as the two inputs of a compact and low power comparator. The floating node voltage V_G discharges, when its gate voltage exceeds the MN2 source voltage by a V_{TH}. The node V_G modulates the ON/OFF of the OLED anode output voltage V_{Anode}. The row ramp signal V_{Ramp} is a downward ramp which resets to the maximum level at the end/start of each ramp cycle. The time for V_{Ramp} to decrease from the maximum level to V_C-V_{TH} is the OFF time for a ramp cycle. After that, the ON time is from V_C-V_{TH} to the minimum. The width of the generated pulse is proportional to the level of V_C. Gamma correction is realised by reshaping the ramp signal.

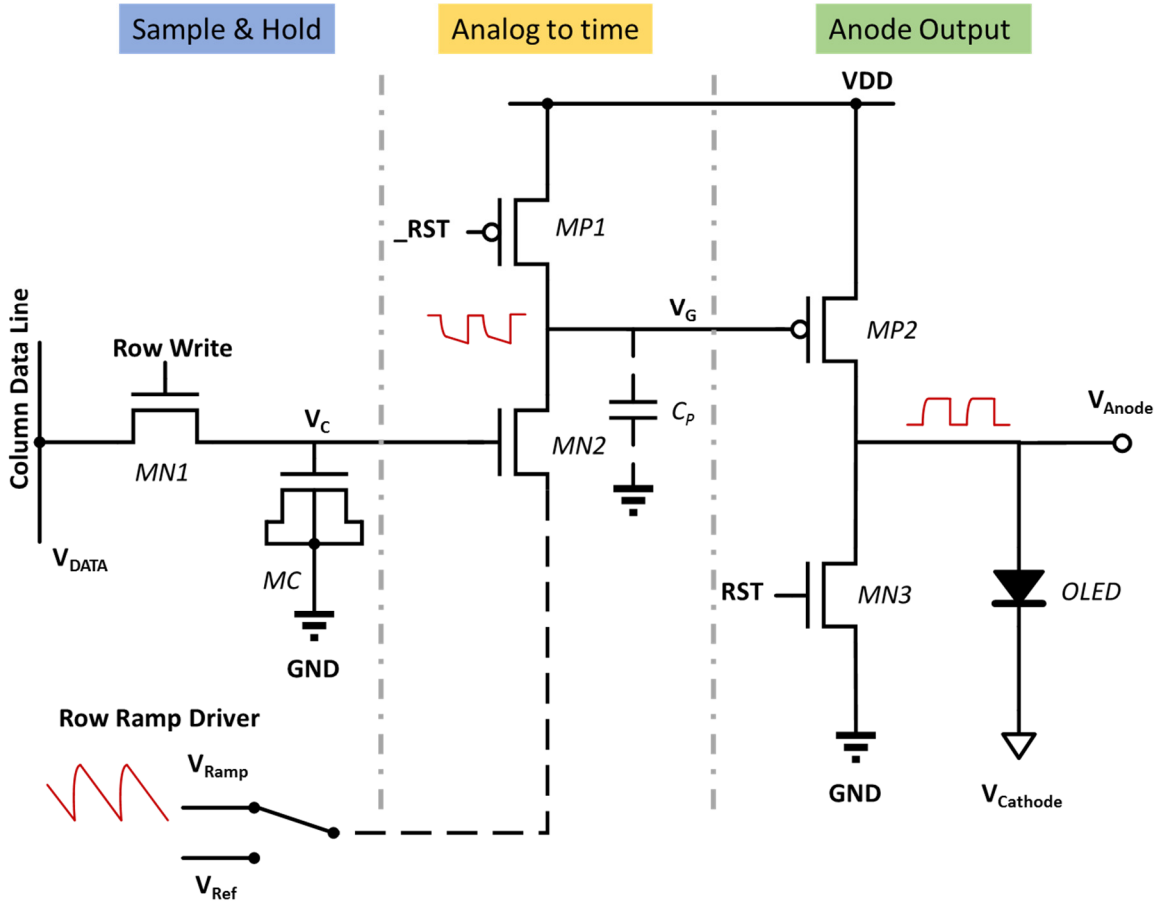


Figure 3-20 Schematic of the 5T1C PWM pixel

The analogue to time conversion is an inverted version of a time-to-analogue converter (TAC). [169, 170] have shown an example TAC pixel for SPAD TCSPC (time-correlated single photon counting) sensors. The arrival of a photon triggers the TAC pixel to sample a voltage from the ramp signal. The sampled voltage represents the time of arrival of the photon. The analogue voltage is then converted to the time of the photon arrival.

3.5.2.2 Timing diagram

The timing diagram of the analogue PWM pixel is shown in Figure 3-21 (a). Each row of pixels is written once in every display frame. The frame starts after the Write phase of a pixel, and last until the pixel is being addressed again. The RST (reset) signal is synchronous to the falling Ramp signal. There are two modes for the pixel addressing scheme. The first is a global shutter mode. All the pixels are addressed at the beginning of the frame as shown in Figure 3-21 (b). The emission phase follows the addressing phase. The second is a rolling address mode. The pixels are addressed row by row during the emission phase of each frame, as in Figure 3-21 (c). The reset signal is applied individually for each row. It is also activated when the row of pixels are being addressed.

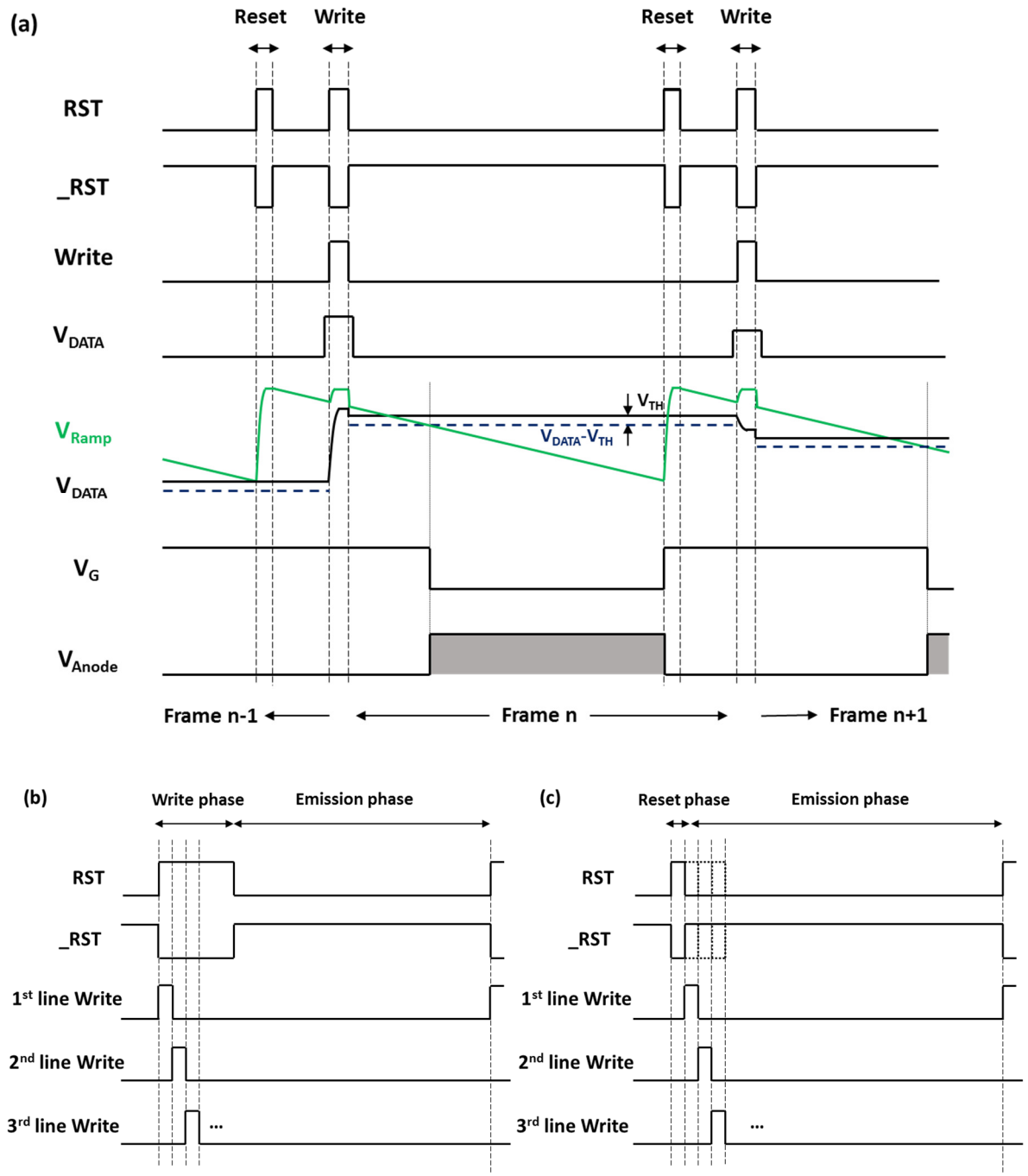


Figure 3-21 (a) analogue PWM pixel timing diagram; Pixel array addressing scheme (b) global shutter mode (c) rolling mode

Both RST and Ramp are reset (high) at the start/end of the ramp cycle. During the reset phase (Figure 3-22(a)), the internal node V_G is charged to VDD to turn off MP2, and the V_{Anode} output is set low to turn off the OLED. The Ramp signal is set to a voltage higher than the maximum level of V_{DATA} (V_{Ref}>V_{DATA}) to clamp MN2 in the cut-off region.

If the pixel array is configured in global shutter mode, the pixel is addressed during the reset phase. Otherwise, it is addressed during the emission phase. When a pixel is being addressed, as shown in Figure 3-22(b), both the Write signal and RST signal are activated. Both source and drain terminals of MOSFET MN2 are reset to a known voltage. This assures V_C is charged up to a consistent fixed level without the effect from V_G and V_{Ramp} coupling through the gate-source and gate-drain capacitance of MN2.

Figure 3-22 (c) shows the pixel array operation in the emission phase. Once the reset phase finished and it is not being addressed, the Ramp signal starts to decay after the reset phase. When V_{Ramp} decreases to less than V_C-V_{TH} (V_{TH} of M2), the charge stored on the gate of MP2 will discharge through MN2. The internal node V_G is charged to V_{Ramp}. As discussed in section 3.4.1, for V_{Ramp} <V_{DD}-|V_{TH}|, the PMOS is likely in the triode operation region. The pixel OLED anode voltage switches from GND to VDD.

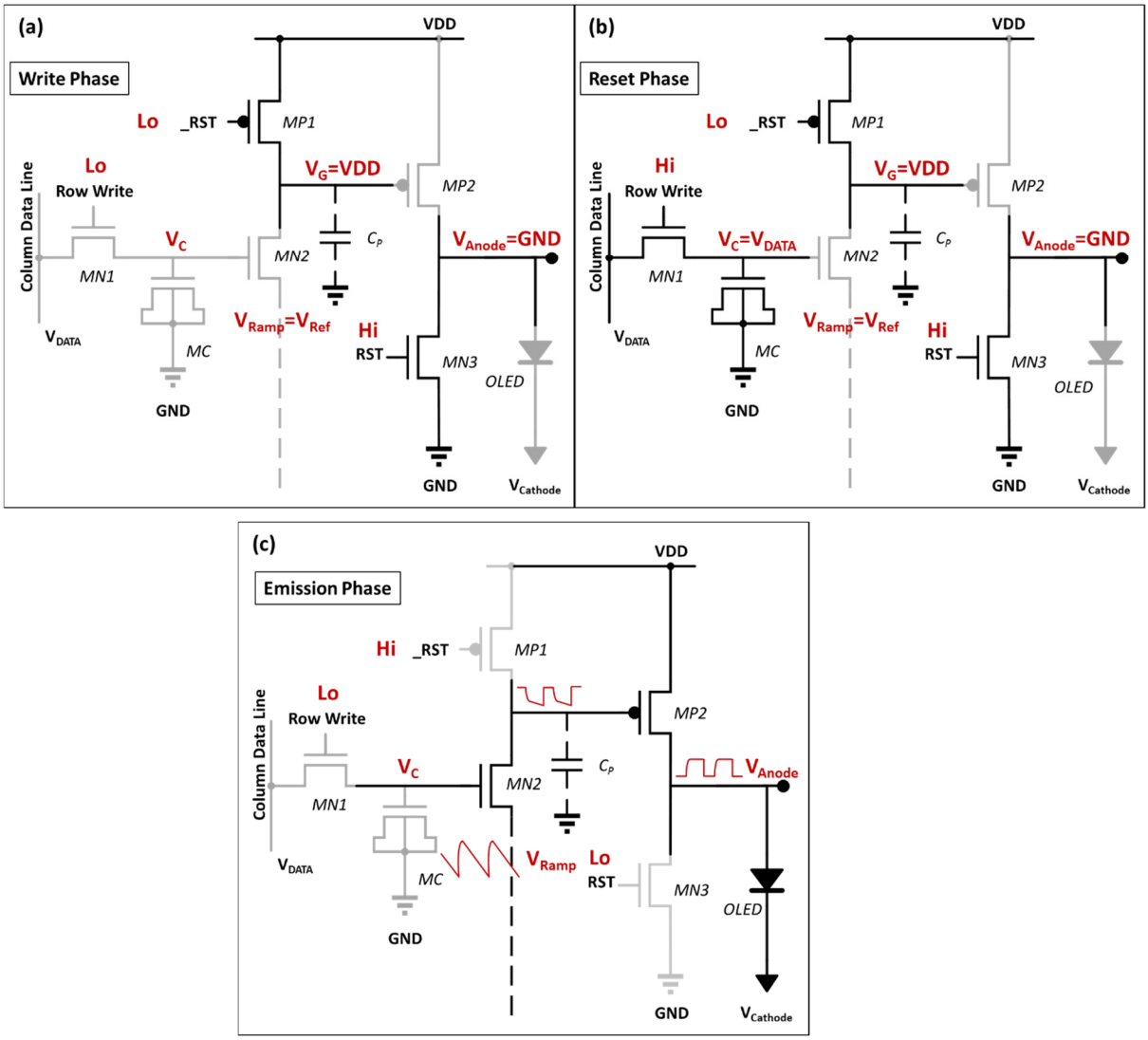


Figure 3-22 Analogue PWM pixel operation (a) Write phase (b) Reset phase (c) Emission phase

Figure 3-23 illustrates a transient simulation of the analogue PWM pixel. The simulated frame period is 20 ms (50 Hz). Both V_{Ramp} and RST reset at the start of a ramp period. The Ramp reset voltage V_{Ref} is set as VDD. The reset pulse width is 2 µs. The Write phase starts at 2 ms after the reset phase. The Write phase lasts for 2 µs. A V_{DATA} of 1.8 V is stored on V_C (1.705 V after MN1 switched off due to charge injection). The ramp signal decays from 2 V to 1 V each cycle. The OLED anode current crosses 5.63 nA (half I) at 15.61 ms of each frame. At the time when I_{Anode} is switching, V_{Ramp} is at 1.2 V, and V_G discharge from 4.8 V to 4.37 V. The gate-source voltage difference is about 0.46 V, slightly less than the V_{TH} of MN2. The subthreshold current is enough to discharge the node V_G.

For the sample and hold stage (MN1, MN2, MC), according to the previous simulation (Figure 3-14 (b)), the capacitance of MOS capacitor is consistent for the input V_{DATA} higher than V_{TH}. The similar charge injection and clock feedthrough simulation for the 2T SF pixel (Figure 3-17) is performed. As shown in Figure 3-24, for $V_{DATA} < 0.7$ V (V_{TH}), the level of charge injection (ΔV) varies for a significant amount. It is due to the sharp increase of MOS capacitance at V_{TH}. For $V_{DATA} > 0.7$ V, the charge injection and clock feedthrough voltage drop decrease consistently with V_{DATA} which is close to the theoretical Equation 3-4.

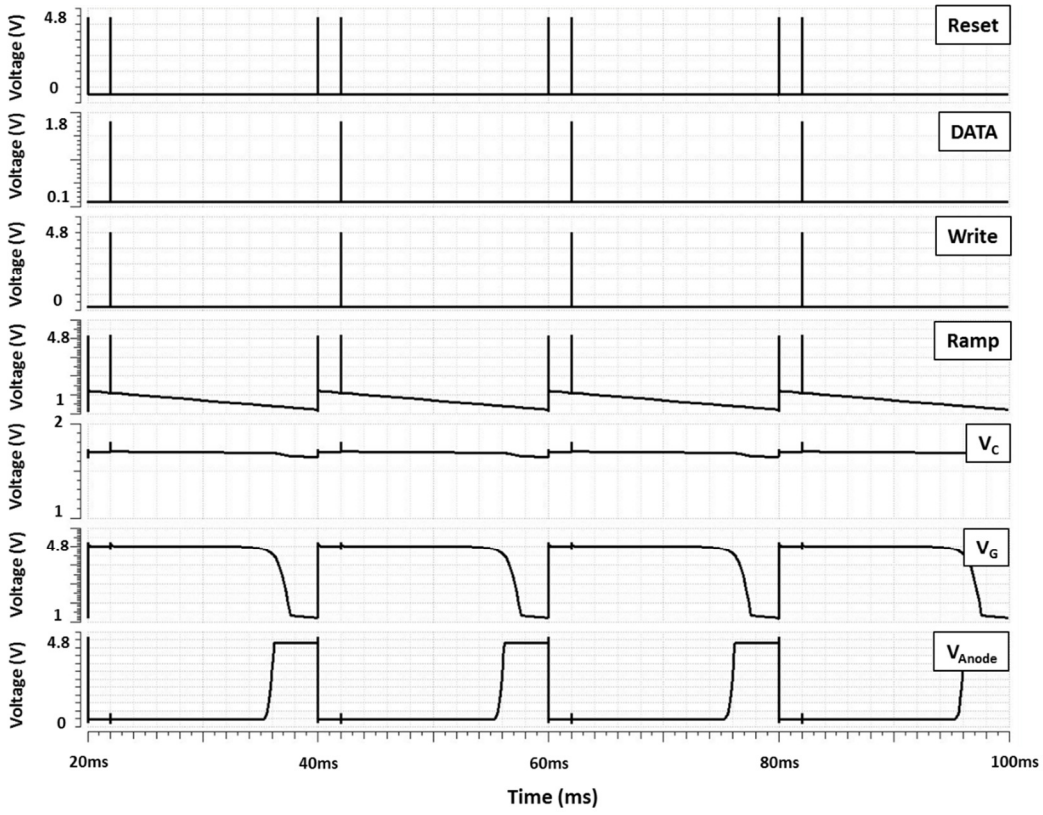


Figure 3-23 Transient simulations of the analogue PWM pixel.

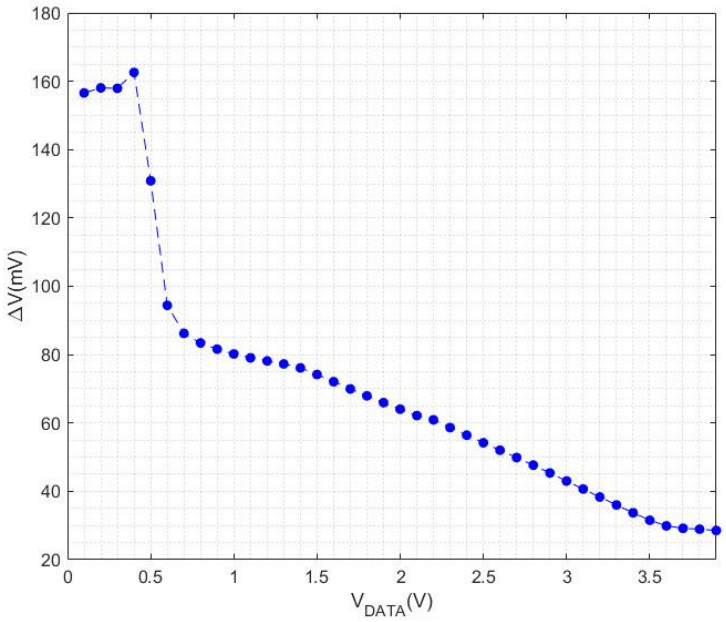


Figure 3-24 the amount of charge injection and clock feedthrough (ΔV) versus V_{DATA} for the analogue PWM pixel

3.5.2.3 Ramp driver for improving linearity

As we discussed above, the V_{GS} of MN2 is 0.46 V, when the V_{GS} of MP2 switch on the anode OLED current from OFF to ON (at half I_{Anode}). It is the subthreshold current of MN2 that is enough to switch on the OLED. The subthreshold (also known as weak-inversion) drain current is generated by the diffusion of minority carriers. It increases exponentially with the gate-source voltage [171, 172],

$$I_D = \mu_n C_d \frac{W}{L}\left(\exp\frac{V_{GS}-V_{TH}}{\zeta V_T}\right)\left(1-\exp\frac{-V_{DS}}{V_T}\right),$$

$$\zeta \approx 1+\frac{C_d}{C_{ox}},$$

$$C_d = \sqrt{\frac{\varepsilon_{Si} q N_A}{-4\phi_p}} \qquad \textbf{Equation 3-7}$$

$$V_{TH} = V_{FB} - 2\phi_p + \frac{\sqrt{2\varepsilon_{Si} q N_A\left(-2\phi_p - V_{BS}\right)}}{C_{ox}}$$

Where C_{ox} is the gate oxide per unit area; V_T is the thermal voltage (kT/q), about 25.6mV in room temperature; C_d is the capacitance of the depletion region under the gate area; ϕ_p is the P-substrate

electrostatic potential as in Equation 3-6; N_A is the concentration of acceptor atoms; ε_{Si} is the silicon dielectric constant.

For a high-level V_{DS} (larger than a few V_T), Equation 3-7 is dominated by the effect of V_{GS}, as $\exp\frac{-V_{DS}}{V_T}$ becomes negligible. The amount of charge that discharge/charge from the node V_G can be described as an integration of the subthreshold current over time. Among the components of the subthreshold current, only V_{Ramp} varies[26] with time before V_G discharging further. V_{Ramp} is a periodic signal of time. The subthreshold current is negligible for V_{GS}<0. So the integration can be calculated starting from $V_{Ramp} = V_C$. The among of accumulated charge can be described as,

$$v_{Ramp}(t) = V_{Ramp_{max}} - \frac{V_{Ramp_{max}} - V_{Ramp_{min}}}{T} \cdot t,$$

$$Q(\tau) = \int_{\tau_0}^{\tau} I_D dt = \int_{\tau_0}^{\tau} \mu_n C_d \frac{W}{L}\left(\exp\frac{\Delta V\left(V_{Ramp}(t)\right)V_{GS}}{\zeta V_T}\right)dt$$

$$= \frac{T}{V_{Ramp_{max}} - V_{Ramp_{min}}}\int_{V_{Ramp}}^{V_C} \mu_n C_d \frac{W}{L}\left(\exp\frac{\Delta V\left(v_{Ramp}\right)}{\zeta V_T}\right)dv_{Ramp}\,, \qquad \textbf{Equation 3-8}$$

$$\Delta V = V_{GS} - V_{TH} = V_C - V_{Ramp} - V_{FB} + 2\phi_p - \frac{\sqrt{2\varepsilon_{Si}qN_A\left(-2\phi_p + V_{Ramp}\right)}}{C_{ox}},$$

Where $v_{Ramp}(t)$ is the ramp transient function; τ_0 is moment $V_{Ramp} = V_C$; $V_{Ramp_{max}}$ is the maximum V_{Ramp}; $V_{Ramp_{min}}$ is the minimum V_{Ramp}; T is the ramp/display frame period.

There is no indefinite integral solution for $\int \exp\left(\Delta V\left(V_{Ramp}\right)\right) dV_{Ramp}$. The integration in Equation 3-8 needs a special function (i.e. Gauss error function) to be resolved numerically. The V_{Ramp} component in V_{TH} is the cause of nonlinearity to ΔV. Therefore, we designed a source follower buffer to apply the same V_{TH} shift to compensate the V_{Ramp}, as shown in Figure 3-25. The Ramp signal, which is generated externally, is buffered by a current bias source follower. The bias current is generated on the PCB and copied to bias the source follower with a current mirror.

[26] Assume the leakage on V_C at the gate terminal is negligible. There is no correlation between V_C and time

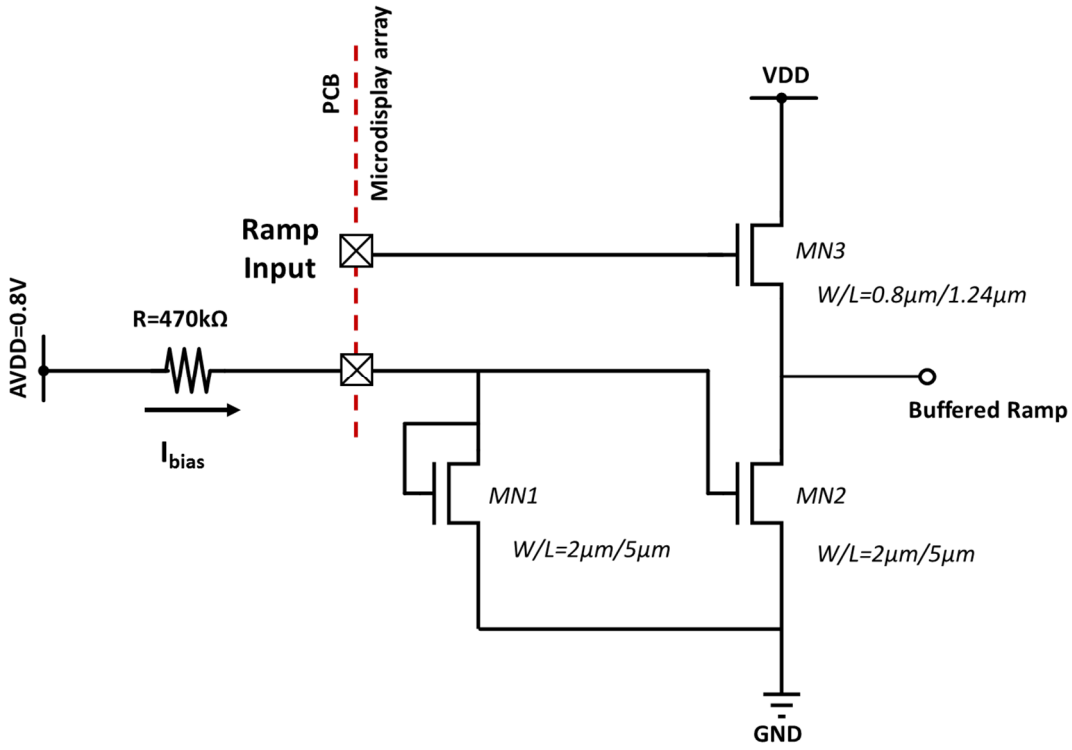


Figure 3-25 source follower buffer for V_{Ramp}

The buffered ramp signal is,

$$I_{bias} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{Ramp} - V_{Ramp_{buf}} - V_{TH_{buffer}}\right)^2$$

$$V_{Ramp_{buf}} = V_{Ramp} - V_{TH_{buffer}} - \sqrt{\frac{2I_{bias}}{\mu_n C_{ox}}\cdot\frac{L}{W}}$$

Equation 3-9

$V_{TH_{buffer}}$ is the threshold voltage for MN3. The transistor MN3 in Figure 3-25 is the same size as the comparator transistor MN2 in Figure 3-20. The buffered ramp signal will apply to the source terminal of MN2 in each pixel. Since both transistors are of same size and same source voltage, it can assume the values of both V_{TH} are the same. The ΔV in Equation 3-8 is simplified,

$$V_{TH\_buffer} = V_{TH\_MN2},$$

$$\begin{aligned}\Delta V &= V_C - V_{Ramp_{buf}} - V_{TH_{MN2}}\\ &= V_C - V_{Ramp} + V_{TH_{buffer}} + \sqrt{\frac{2I_{bias}}{\mu_n C_{ox}}\cdot\frac{L}{W}} - V_{TH_{MN2}}\\ &= V_C - V_{Ramp} + \Delta V_{I_{bias}},\end{aligned}$$

Equation 3-10

$$\Delta V_{I_{bias}} = \sqrt{\frac{2I_{bias}}{\mu_n C_{ox}} \cdot \frac{L}{W}},$$

The quantity of accumulated charges on the node V_G is,

$$\begin{aligned} & Q(V_{Ramp}) \\ &= \frac{T}{V_{Ramp_{max}} - V_{Ramp_{min}}} \int_{V_{Ramp}}^{V_C} \mu_n C_d \frac{W}{L} \left(\exp \frac{V_C - V_{Ramp} + \sqrt{\frac{2I_{bias}}{\mu_n C_{ox}} \cdot \frac{L}{W}}}{\zeta V_T} \right) dv_{Ramp} \\ &= \frac{T \cdot \zeta V_T}{V_{Ramp_{max}} - V_{Ramp_{min}}} \mu_n C_d \frac{W}{L} \left(\exp \frac{V_C - v_{Ramp} + \sqrt{\frac{2I_{bias}}{\mu_n C_{ox}} \cdot \frac{L}{W}}}{\zeta V_T} \right) \Bigg|_{V_C}^{V_{Ramp}} \\ &= \frac{T \cdot \zeta V_T \cdot \mu_n C_d \cdot W}{\left(V_{Ramp_{max}} - V_{Ramp_{min}}\right) \cdot L} \exp \frac{\sqrt{\frac{2I_{bias}}{\mu_n C_{ox}} \cdot \frac{L}{W}}}{\zeta V_T} \left[\exp \frac{V_C - V_{Ramp}}{\zeta V_T} - 1 \right], \end{aligned}$$

Equation 3-11

If ΔQ is the amount of charge that V_{GS} of MP2 is enough to turn on the OLED (OLED anode current cross half), the Ramp signal voltage when OLED switch on is,

$$\Delta Q = \frac{T \cdot \zeta V_T \cdot \mu_n C_d \cdot W}{\left(V_{Ramp_{max}} - V_{Ramp_{min}}\right) \cdot L} \exp \frac{\sqrt{\frac{2I_{bias}}{\mu_n C_{ox}} \cdot \frac{L}{W}}}{\zeta V_T} \left[\exp \frac{V_C - V_{Ramp_{sw}}}{\zeta V_T} - 1 \right],$$

$$\exp \frac{V_C - V_{Ramp_{sw}}}{\zeta V_T} = \frac{\Delta Q \cdot \left(V_{Ramp_{max}} - V_{Ramp_{min}}\right) \cdot L}{T \cdot \zeta V_T \cdot \mu_n C_d \cdot W} \exp \left(- \frac{\sqrt{\frac{2I_{bias}}{\mu_n C_{ox}} \cdot \frac{L}{W}}}{\zeta V_T} \right) + 1, \qquad \textbf{Equation 3-12}$$

$$V_{Ramp_{sw}} = V_C - \zeta V_T \ln \left(\frac{\Delta Q \cdot \left(V_{Ramp_{max}} - V_{Ramp_{min}}\right) \cdot L}{T \cdot \zeta V_T \cdot \mu_n C_d \cdot W} \exp \left(- \frac{\sqrt{\frac{2I_{bias}}{\mu_n C_{ox}} \cdot \frac{L}{W}}}{\zeta V_T} \right) + 1 \right),$$

Thus, the ramp switch voltage $V_{Ramp_{sw}}$ is a linear function of V_C stored in-pixel with the ramp signal buffered by a source follower. Figure 3-26 shows the simulation result of the V_{Ramp} switch voltage with a sweep of V_{DATA}. Both simulations with and without the source follower buffer are performed. The non-buffer ramp signal is sweep between 1 V and 2 V. A linear characteristic curve with a slope of 0.8155 is obtained. The regression fits for V_{DATA} range of 1.55 V and 2.7 V with $R^2 > 0.999$. However,

it is not a deterministic value from derivation. The theoretical curve are likely to be non-linear, but the non-linearity is small for low source voltages which is V_{Ramp}.

For the buffered Ramp signal, a 2 V – 3 V ramp is input through the source follower buffer. The valid range V_{DATA} is between 1.5 V and 2.5 V. The regressed slope is 1.007, slightly higher than the theoretical value – one from Equation 3-12. One possible cause of a more than one slope could be the charge injection. According to Equation 3-4, the stored V_C has a slope of $\left(1+\frac{WLC_{ox}}{2C_{S1}}\right)$ regarding to V_{DATA}. The y-intercept value can be adjusted by the I_{bias}.

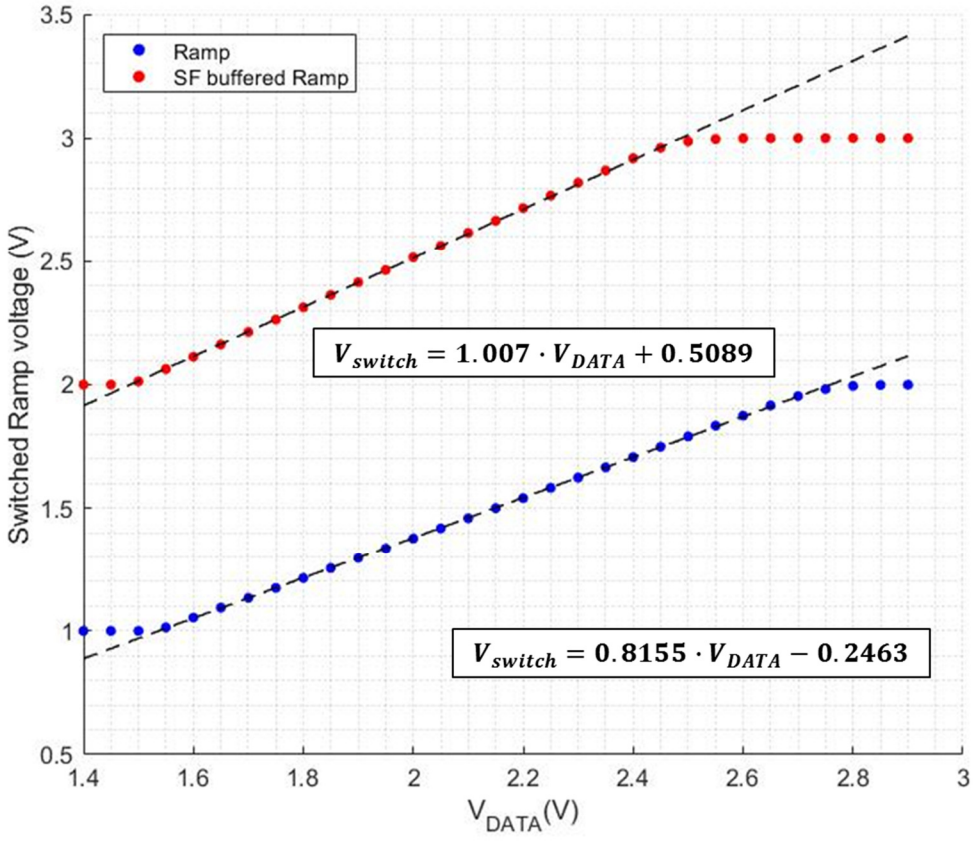


Figure 3-26 simulations of the Ramp switch voltage versus input V_{DATA}

3.5.2.4 MOSFET sizing and layout design

There are two PMOS and four NMOS MOSFETs (one for MOS cap) each pixel. As the pixel composes both NMOS and PMOS, additional area is consumed for the N-well spacing design rules. The N-well spacing can be shared by PMOS transistors across multiple pixels locally. Figure 3-27 shows an option of a 2×2 or 'quad' well-sharing structure. In this case, there is no independent bulk voltage control for each PMOS, but the utilisation of the pixel area is maximised.

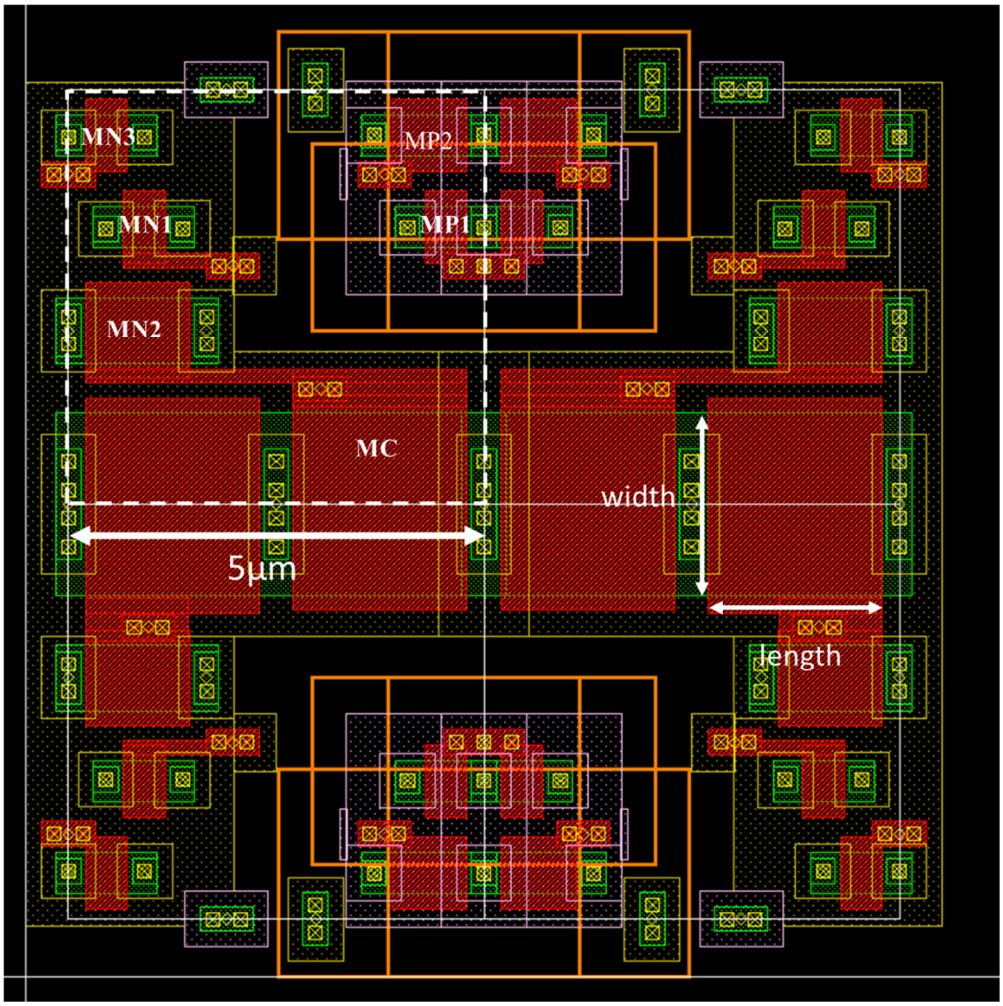


Figure 3-27 analogue PWM pixel layout

As shown in Figure 3-27, all the MOSFETs need to be with the same orientation for the reason of size matching. The MN1, MN3 and MP1 are MOSFET switches with minimum size transistors W/L=0.5 µm / 0.5 µm. The sizing of the MOS cap and the switch transistor are critical for the pixel performance. Size of MOS cap determines the level of leakage flicker of V_C over a display period. The larger is the MOS cap, the longer it can maintain the value of V_C. The size of the MN2 transistor is critical for the mismatch of transistor's V_{TH} and mobility which affects the ramp switch voltage calculated in Equation 3-12. With drain and source shared with the MC transistors of peripheral pixels, the utmost length for MC is 2.08 µm. The length of MN2 is constraint by the spacing design rule of N-well. The greatest possible length of MN2 is 1.24 µm. On the other hand, there is a trade-off between the width of MC and MN2. The sum of the MC and MN2 width is a fixed value – 3 µm. Figure 3-28 (a) shows a simulation of the correlation between the width of the MC cap and storage V_C leakage. The leakage is measured for a 2.1 V V_{DATA} input in a 10 ms frame. As the capacitance is proportional to the size of MC, the magnitude of leakage decreases with the width. To evaluate the level of mismatch, a 100× Monte Carlo simulation is performed for various the width of MN2 between 0.5 µm and 1 µm. A standard variation of the average current over a display frame is plotted in Figure 3-28 (b). The current is measured for a

2.1 V V_{DATA} input with a non-buffered V_{Ramp} between 1V and 2V. The resulting pulse width is about half the period. The mean value for the average current across different width is 5.457nA (0.5µm), 5.44nA (0.6µm), 5.429nA (0.7µm), 5.426nA (0.8µm), 5.426nA (0.9µm) and 5.426nA (1µm) with I_{ON}=11.24nA.

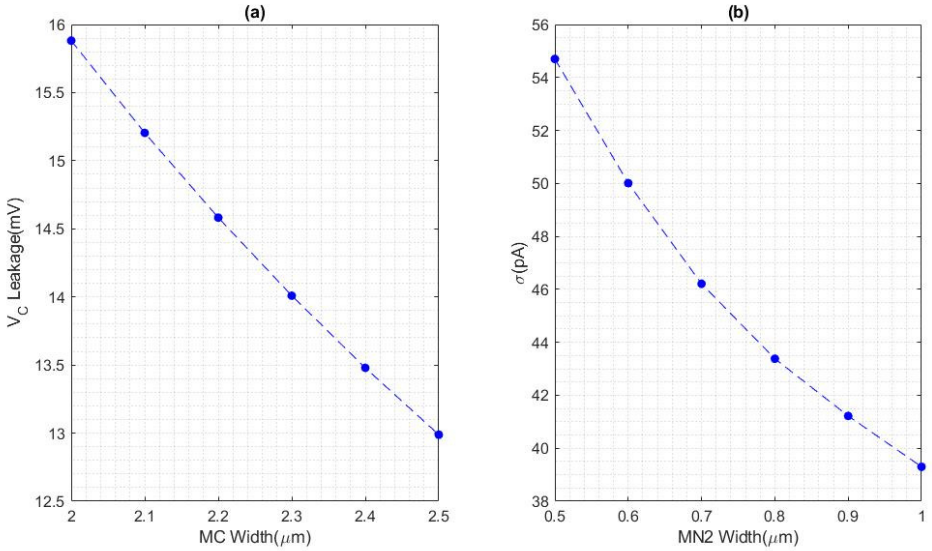


Figure 3-28 (a) V_C leakage versus width of transistor MC (input V_{DATA}=2.1V) (b) 100× Monte Carlo simulation standard deviation of average current versus the width of transistor MN2

In Figure 3-28 (b), the slope of standard deviation versus transistor width slows down for a further increase of MN2 width more than 0.8µm. Therefore, to optimise the trade-off between the sizing MC and MN2, the width of MN2 is chosen as 0.8µm and width of MC as 2.2µm. In this case, the 2.2µm×2.08µm results in a 14.58mV leakage which is less than 1.5% of the V_{DATA} range. A 43.38pA standard deviation of average current is acquired. The 3σ range is between 5.332nA and 5.592nA which means 99.8% of pixels falls in a range 2.5% variation of pixel current.

In conclusion, the size of the transistor are specified as Table 3-3. Figure 3-29 shows the simulation of the OLED anode voltage waveforms for a 1000× Monte Carlo simulation runs. A histogram of the average OLED current is plotted in Figure 3-30. A 44.09pA standard deviation is achieved which is slightly higher than the result of the 1000× Monte Carlo simulations.

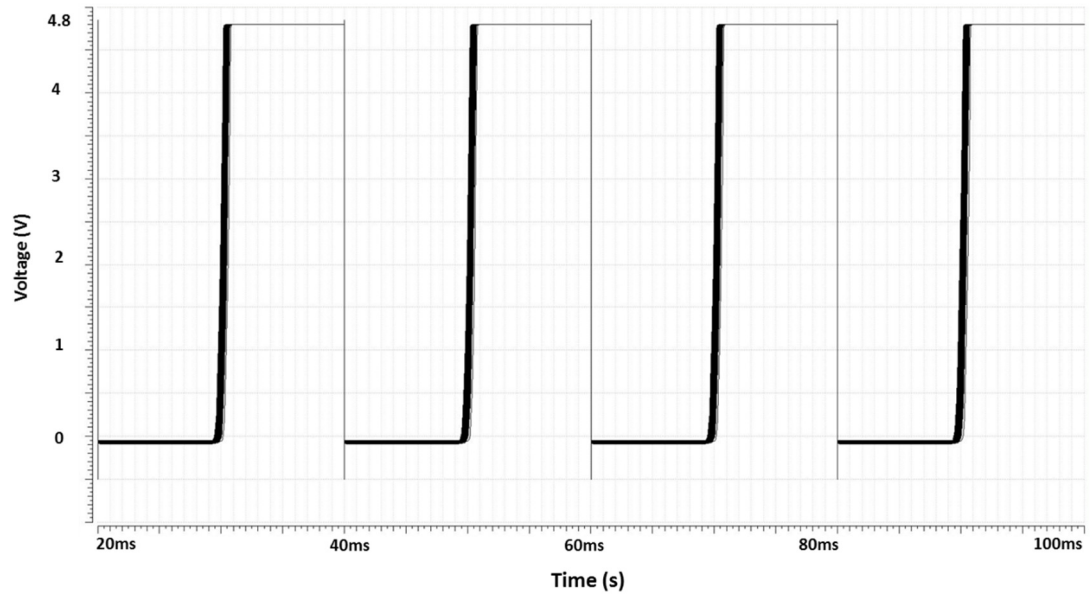


Figure 3-29 Simulation V_{Anode} waveforms for 1000 Monte Carlo runs at typical conditions

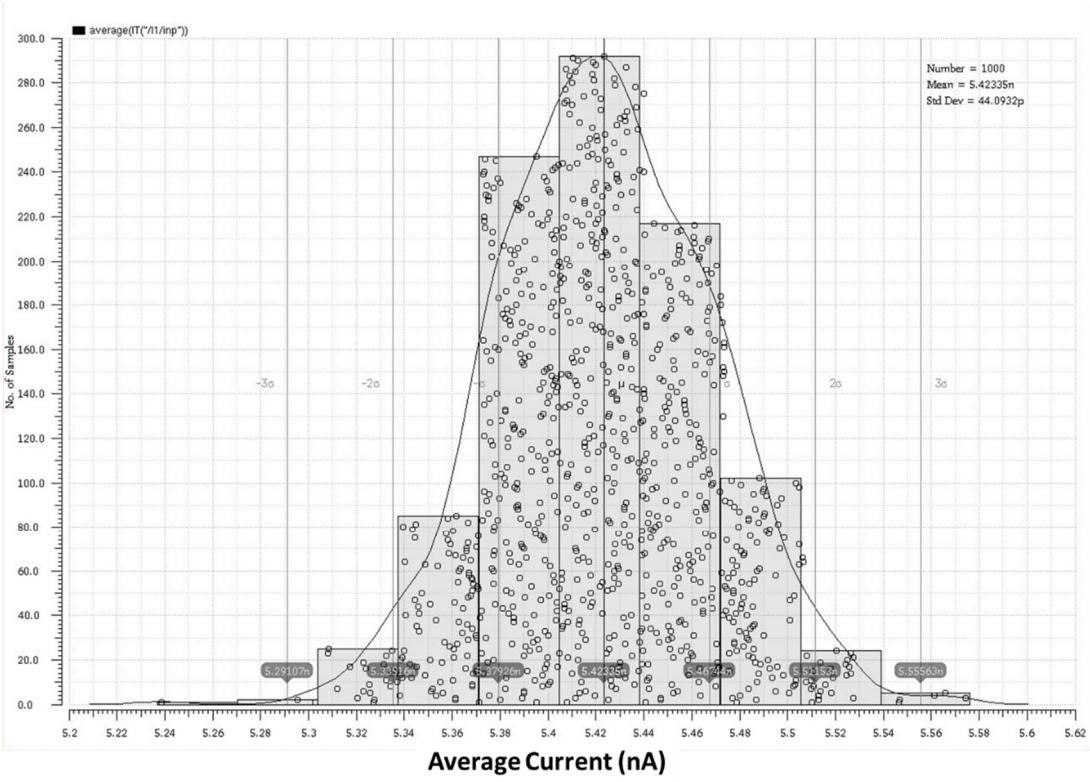


Figure 3-30 histogram of 1000× Monte Carlo simulation of the average pixel current, the x-axis is the average pixel current in nA

Table 3-3 Analogue PWM pixel transistor size

Transistor	Description	Width (µm)	Length (µm)
MN1	DATA input/WR	0.5	0.5
MN2	Comparator transistor	0.8	1.24
MN3	_Reset/V_G pull up	0.5	0.5
MP1	Reset/Output pull down	0.5	0.5
MP2	Output drive transistor	0.5	0.9
MC	Storage MOS cap	2.2	2.08

The same pixel layout is displayed in Figure 3-31 for each of the four metal layers. A large area of metal 1 deposited on top of the MOS cap is wired to ground. The purpose is to add extra MOM capacitance between poly and metal 1 of the storage node V_C. The wire widths of reset, inverted reset and write are chosen to be minimum. The wires V_{Ramp} and V_{DATA} are designed to be wider for reducing the impedance of the metal straps. A large area of VDD and ground for metal 3 and metal 4 is intended for minimisation of the IR drop. The drain and source nodes of the transistors are shielded under the metal layers to reduce the photon-induced leakage. Figure 3-32 shows the layout of two 4×12 analogue PWM pixel arrays including dummy pixels surrounding the arrays. The two arrays are designed separated for electrical testing and optical testing. Hence, the electrical/optical measurement can be performed

independently without any interference. The layout for the ramp control block, generating the reset signal and the ramp switch driver circuits are shown in Figure 3-33.

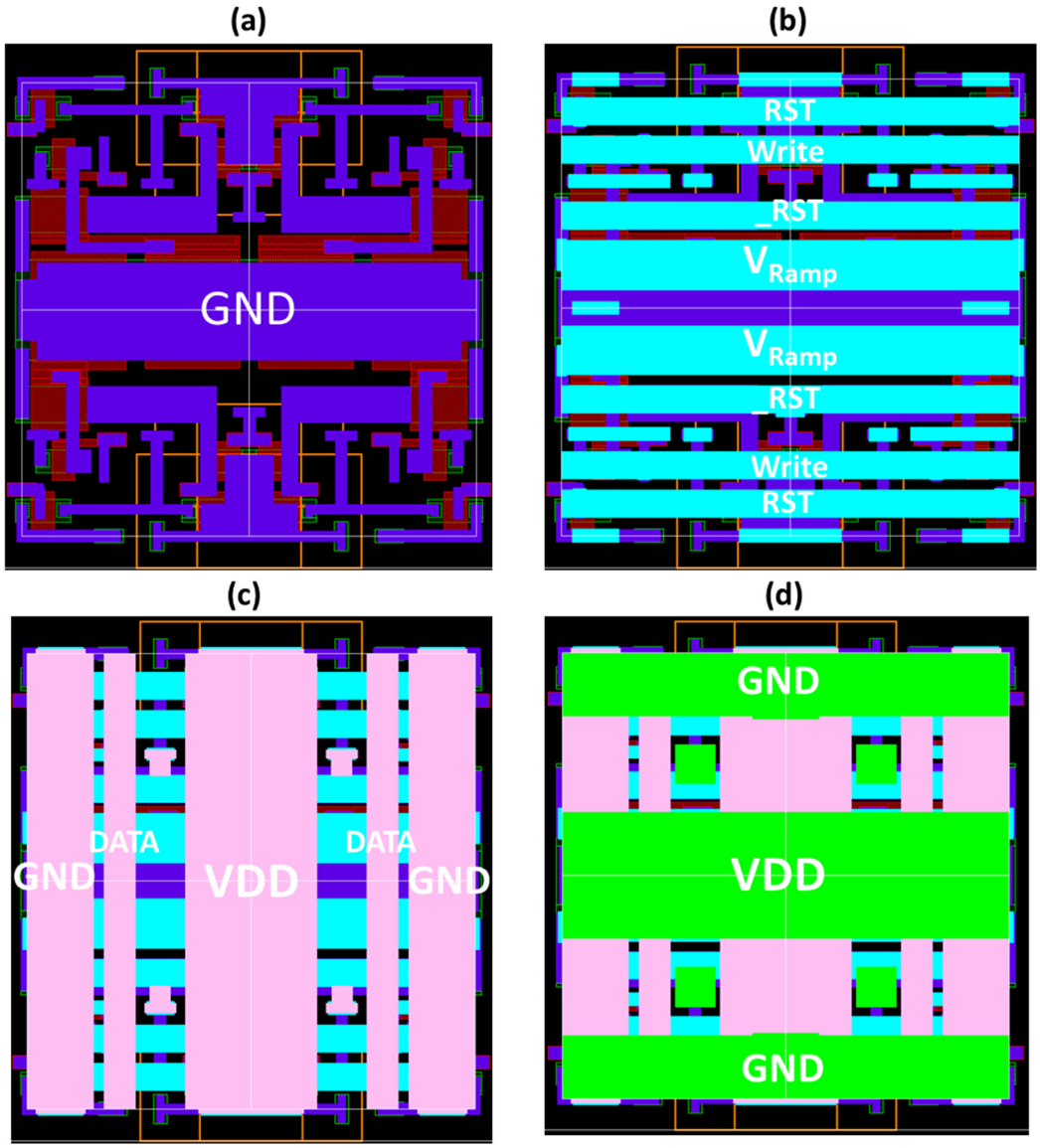


Figure 3-31 Pixel layout showing (a) metal 1, and then incrementally each metal layer (b)-(d) signal wired are indicated

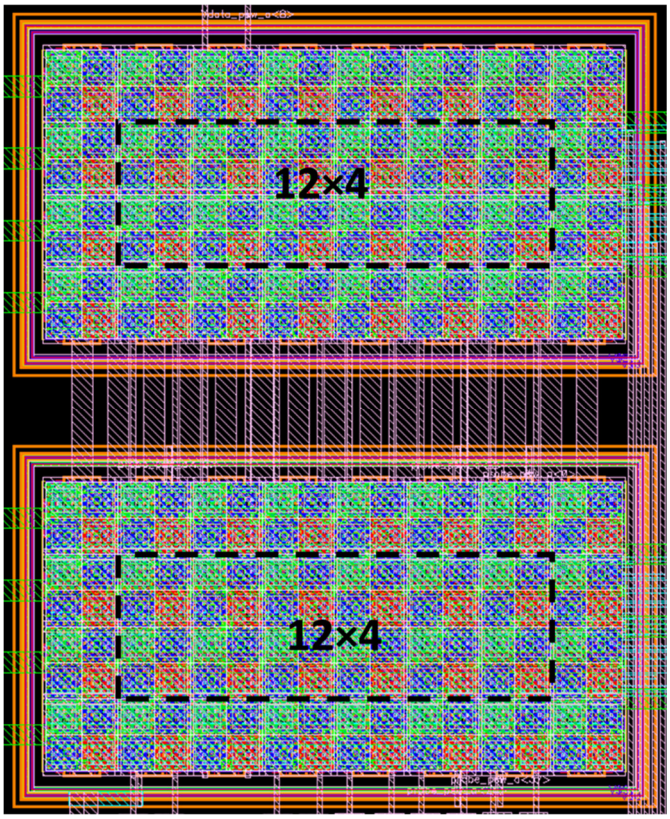


Figure 3-32 layout of the two 4×12 analogue PWM pixel array and the dummy pixels in peripheral, the top array has pixels' anode routed out for electrical measurement, the bottom array for optical measurement

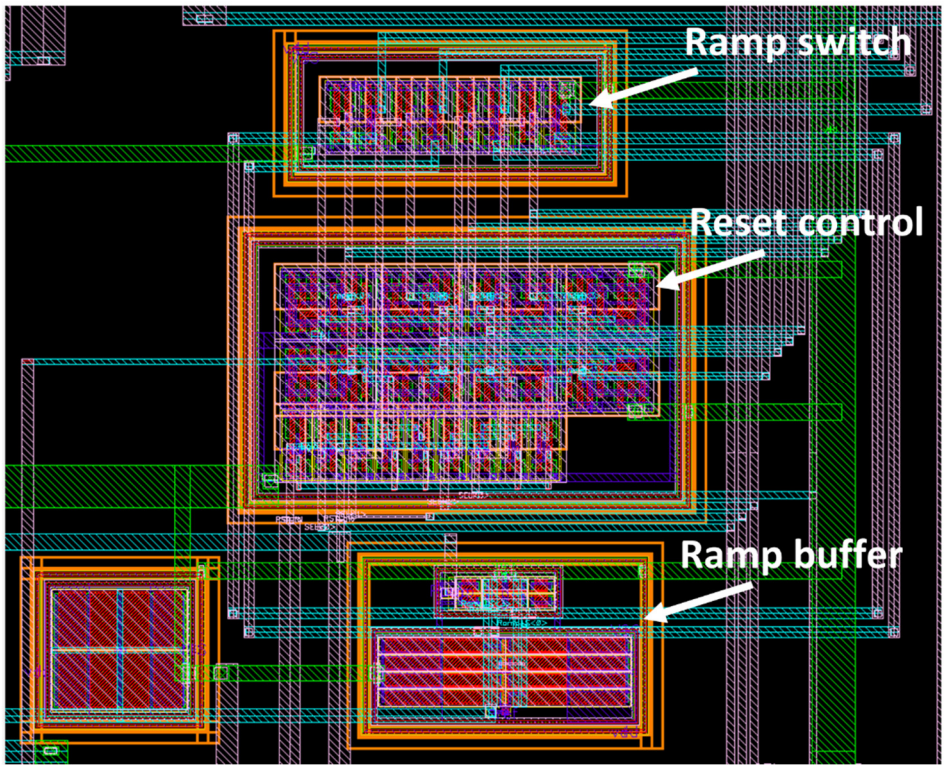


Figure 3-33 Row drivers layout including Ramp buffer, reset control and ramp control switches

3.6 Pixel Characterization

This section details the electrical measurement and analysis of the 2T source follower (with and without annular switch) and the analogue PWM pixel test arrays. The pixel test arrays are characterised with a custom designed PCB with 12-bit DACs[27], an Opal Kelly FPGA card[28], a Lecroy WaveStation signal generator[29] and a Lecroy digital oscilloscope. The DACs on the PCB provide the column DATA voltages. The Opal Kelly card programmes the reset and write signals. Different shape of ramp signal is generated by the signal generator for the analogue PWM pixel. A Keysight B2912A SMU is employed for the measurement of the small-scale pixel current (max ~10 nA per pixel).

3.6.1 2T source follower pixel leakage flicker

Figure 3-34 shows a DC analysis measurement of the 2T SF pixel versus V_{DATA}. The Write signal is set to VDD when the pixel is being addressed. A bias of -6 V is applied to the cathode of the OLED arrays. The electrical measurement is performed for voltage range from 0 to 4.2 V. As the individual pixel current is small, we measure a 4 × 6 pixel array and use the average current as pixel current. However, as shown in Figure 3-34, the average current is about 1 nA for 0 V V_{DATA} which diverges from the simulated I-V curve. As the sum of the 4 × 6 pixel array at 0V V_{DATA} is still a small current (< 1 µA), it is likely the static leakage current from the chip and leakage from the PCB contribute most of the 0 V current. The leakage impedance is

$$R_{leak} = {V_{Cathode}}/{I_{leak}} \cong 6\frac{V}{1}\mu A = 6\ M\Omega \qquad \textbf{Equation 3-13}$$

To remove the influence of the static leakage, the pixel current with the 0 V current removed ($\Delta I = I - I_{0V}$) are also plotted. As shown in Figure 3-34 (right y-axis, blue), the simulated and measured ΔI curves are similar for low voltage. The measured current is higher at high voltages which are likely relating to the pixel edge effect leakage mention in section 2.4.2.

Transient electrical measurements are conducted to evaluate the pixel flicker. The flicker is measured for 40 ms (25 Hz). The switch MOSFET is on for the first 100 µs to allow V_{Anode} settles. During the Write phase, V_{DATA} is switched to 4 V, and V_{DATA} switched to the minimum level following the Write phase when the switch is turned off. The measurement intends to evaluate how long the voltage can be stored in-pixel under the worst case condition – only one row of pixels is emitting.

[27] https://www.analog.com/media/en/technical-documentation/data-sheets/1446fa.pdf
[28] https://opalkelly.com/products/xem6310/
[29] http://teledynelecroy.com/

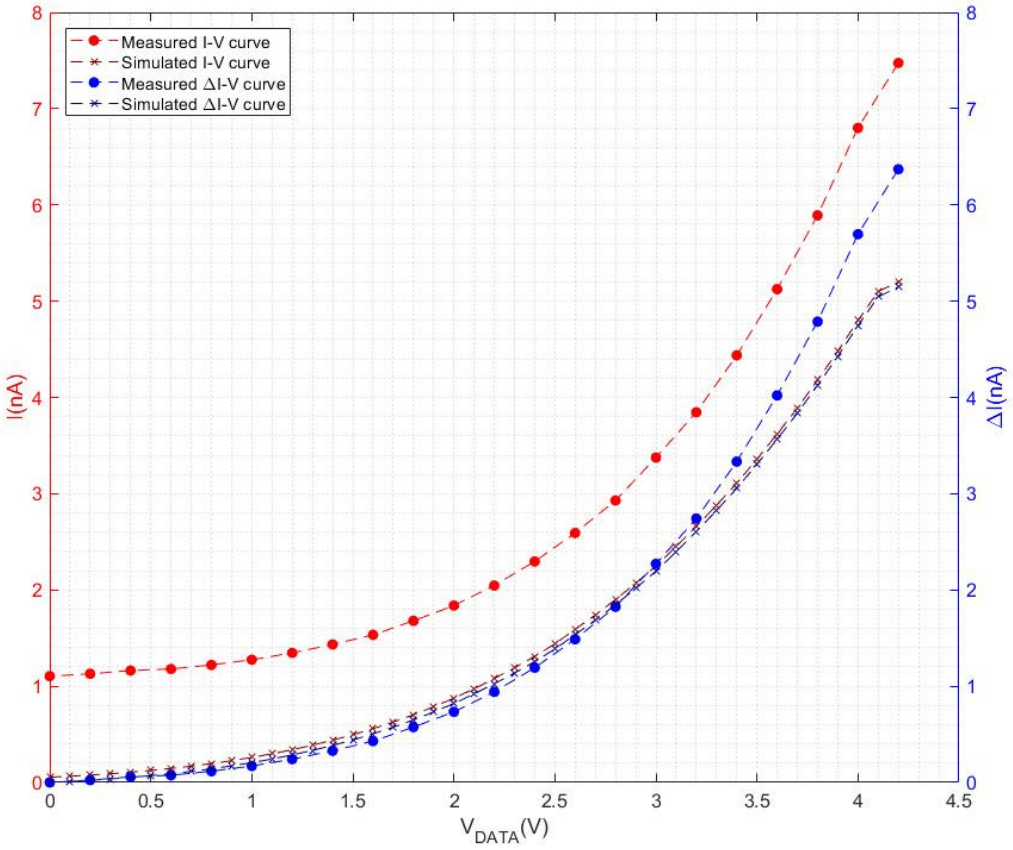


Figure 3-34 Measured and simulated DC analysis of average pixel current versus V_{DATA} The ΔI-V curves has the zero V_{DATA} current deducted to remove static leakage.

The measurement result is plotted in Figure 3-35. As we discussed in section 3.5.1.2, the higher the V_{DATA} minimum level, the less is the leakage flicker. The subthreshold leakage is reduced when V_{GS} is negative. However, it is also evident that V_{Anode} is not settled after the end of the Write phase. The Write phase (0 ~ 100 µs) response is shown in the inset of Figure 3-35. The V_{Anode} curves show charge injection drop after the switch MOSFET turned off. However, it keeps increasing until 3.5V at around 4 ms. The OLED anode terminal is affected by the extra capacitance and resistance of connection wires from the pixel anode to the I/O pad and the oscilloscope probes. Therefore, the anode response could be severely distorted due to the parasitic resistance and capacitance.

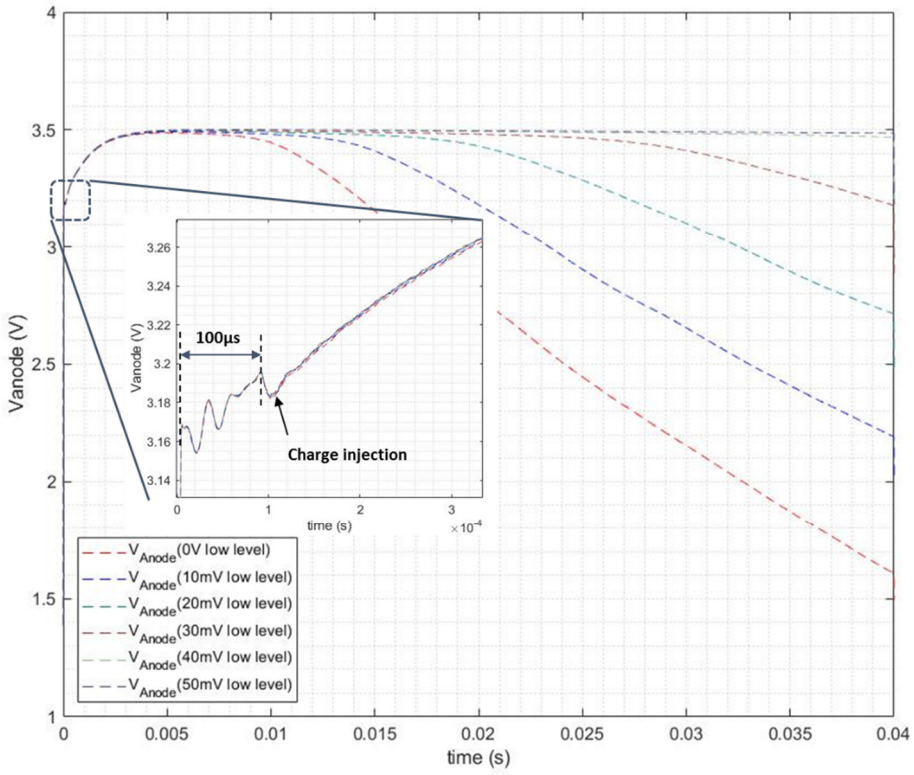


Figure 3-35 Electrical flicker measurement of SF pixel in worst-case leakage with V_{DATA} minimum level as 50 mV, 40 mV, 30 mV, 20 mV, 10 mV and 0 V. The inset shows the temporal response during the Write phase and the charge injection at the end of Write phase.

Electrical measurement can be inaccurate at the pixel level where both the current is tiny. Any electrical noise or parasitic could introduce considerable error. On the other hand, optical measurement is immune from the electrical interferences. The microdisplay pixel-level optical characterisation will be discussed in Chapter 4.

Figure 3-36 shows the V_{Anode} flicker comparison between simulation and measurement. It is measured as the V_{Anode} difference between the end of the 40 ms period and the maximum level. Although both curves follow the same trend as V_{DATA} minimum level increases, the measured electrical leakage is smaller than the simulation. A 40mV minimum V_{DATA} can reduce the leakage to a negligible level.

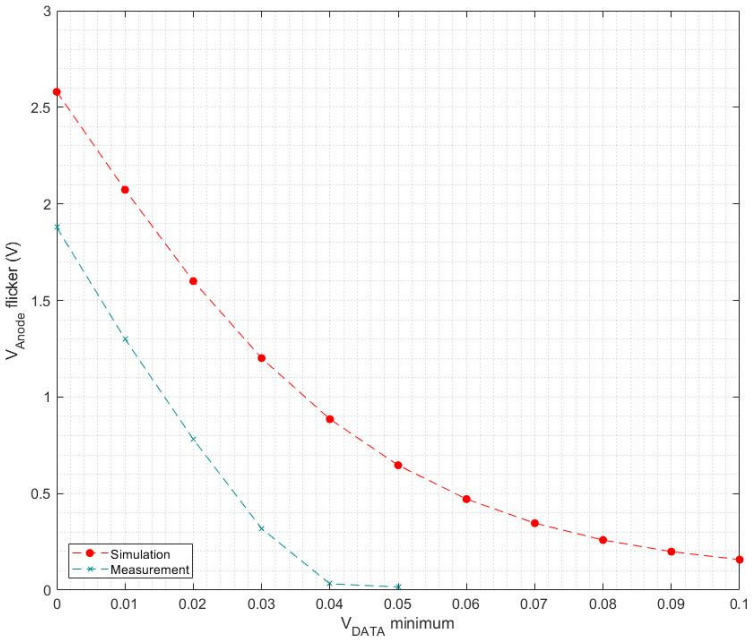


Figure 3-36 the anode voltage flicker vs V_{DATA} minimum level, measurement and simulation

3.6.2 Annular MOSFET improvement on leakage

The same measurement with SF pixel with conventional 2-edge MOSFET has been performed for annular MOSFET pixel. The measured V_{Anode} curves with different V_{DATA} minimum level are shown in Figure 3-37. The leakage induced V_{Anode} flicker decreases with increasing V_{DATA} minimum level. It is also found that the charge injection level is higher compared to conventional MOSFET in Figure 3-35 inset which shows the magnified curve during Write phase. The cause is likely the increased gate area introduce more capacitance for charge injection and clock feedthrough. The empirical extracted size of annular MOSFET is 3.12×0.54 μm^2 which is 6.7 times of the conventional switch.

However, the V_{Anode} curves unexpectedly keep increasing after the switch turned off for both conventional MOSFET and annular MOSFET. For annular MOSFET, V_{Anode} settles at 4.3 ~ 4.4 V (depends on the minimum V_{DATA}) which is higher than the value of V_{DATA} (4 V). The surmise is that the electrically measured V_{Anode} is distorted due to connection wires, I/O pads and the effects from oscilloscope probes. The surmise is confirmed in section 4.7.2 that there is no increase after the switch MOSFET turned off in optical measurements.

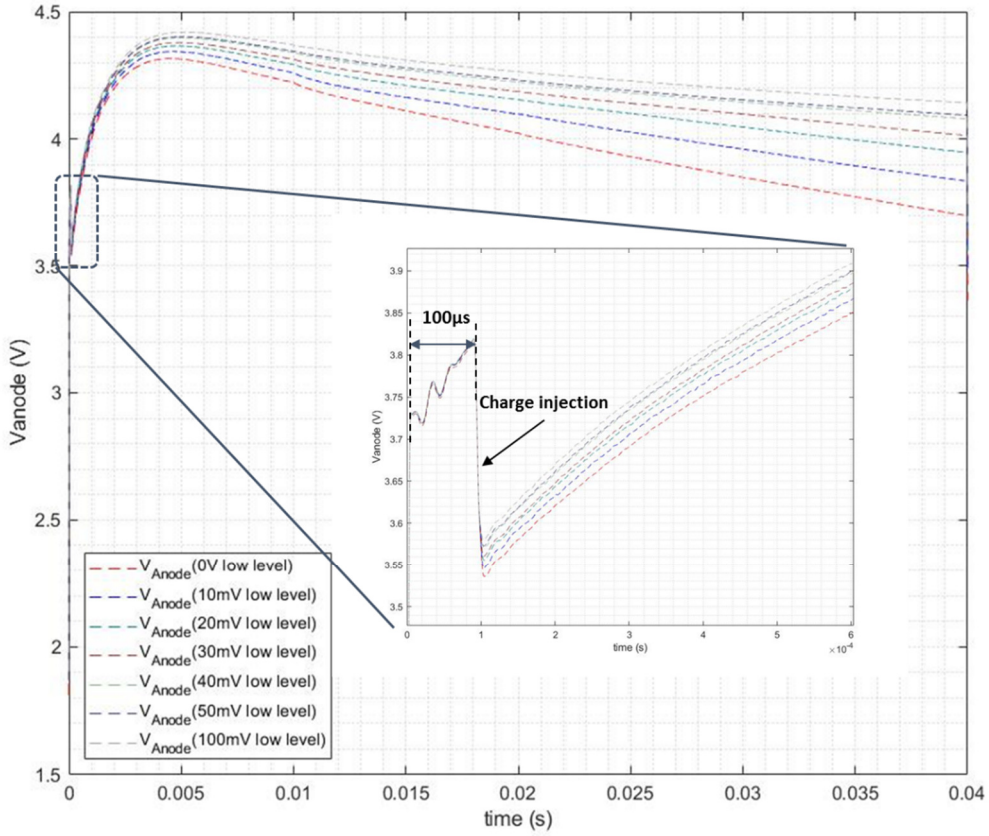


Figure 3-37 Electrical flicker measurement of SF pixel with an annular switch. The worst case V_{DATA} minimum level is 100 mV, 50 mV, 40 mV, 30 mV, 20 mV, 10 mV and 0 V. The inset shows the temporal response during the Write phase and the charge injection at the end of Write phase.

Figure 3-38 shows the leakage comparison of both conventional MOSFET and annular MOSFET. It is measured as the leakage between the maximum level of V_{Anode} and at the end of the 40ms period.

For annular MOSFET, the V_{Anode} flicker is less than that of the conventional MOSFET with low V_{DATA} minimum level. Nevertheless, the greater minimum level of V_{DATA} is not as effective as the conventional MOSFETs to reduce flicker. There are only small difference as the minimum level of V_{DATA} increases. The conventional MOSFET has less leakage with the minimum level of V_{DATA} higher than 30mV.

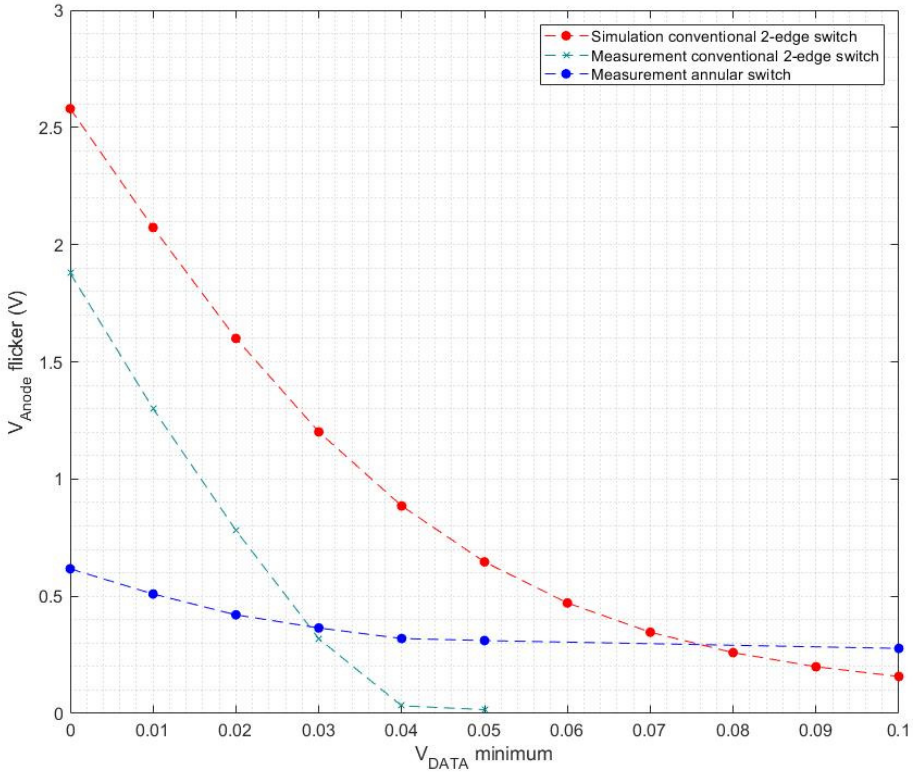


Figure 3-38 the anode voltage flicker vs V_{DATA} minimum level, in simulation for conventional 2-edge MOSFET and measurement for both 2-edge MOSFET (shown in Figure 3-19 (a)) and annular MOSFET (shown in Figure 3-19 (b))

3.6.3 Analogue PWM pixel characterisation

3.6.3.1 Ramp source follower buffer

Before sending the Ramp to the pixel array core, the Ramp signal is buffered by a source follower as shown in Figure 3-25. The electrical measured buffered Ramp is shown in Figure 3-39. The Ramp signal is a 2 V to 1 V down going ramp, generated from an external waveform generator. An external 0.8 V voltage source and a 470 KΩ resistor are used to generate the bias current. The measured Ramp signal is slightly distorted from the simulation.

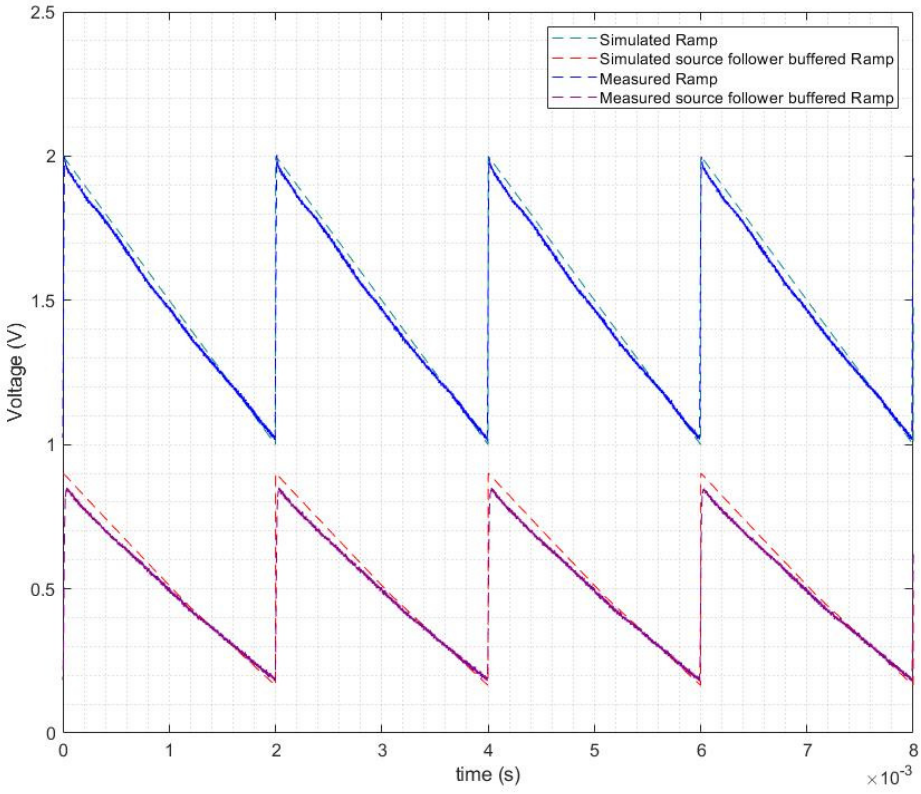
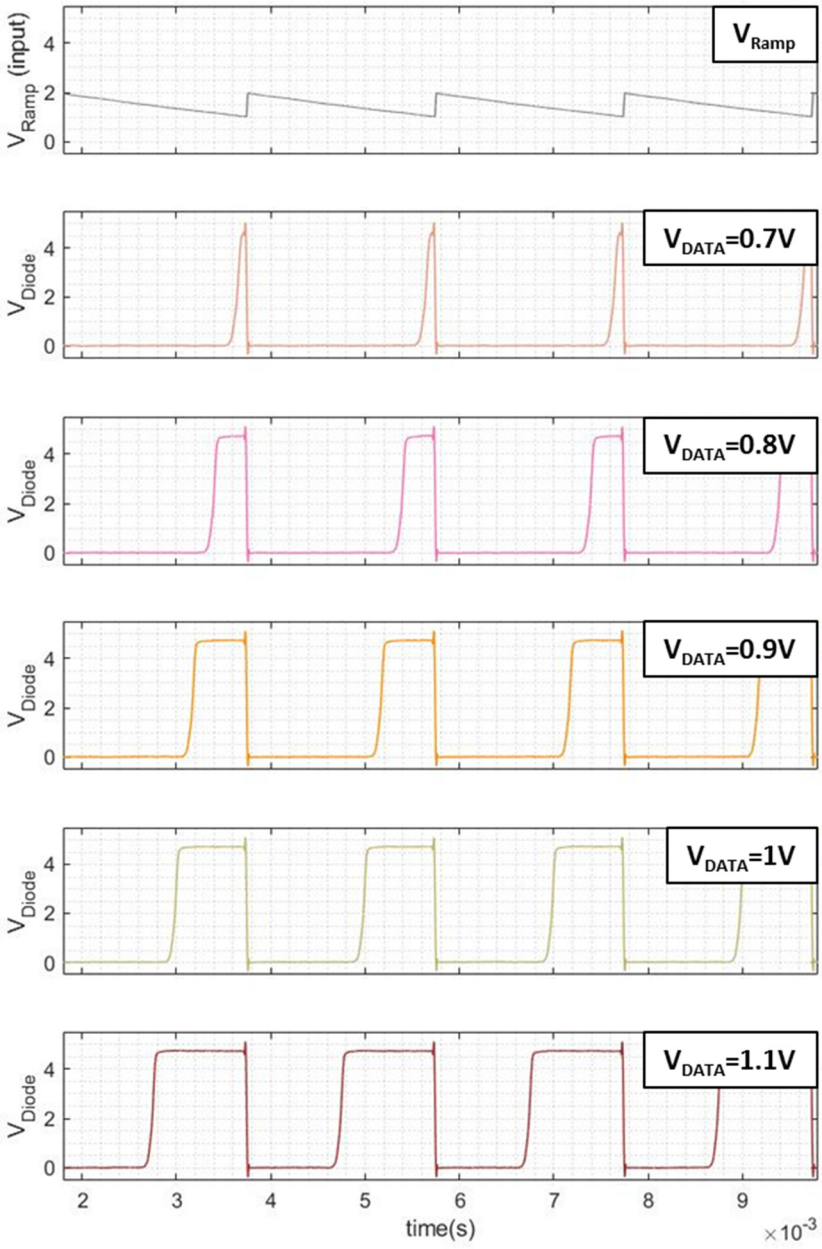


Figure 3-39 Simulated and measured Ramp and the buffered Ramp signal

3.6.3.2 Pulse width generation

The electrical measurement is conducted to evaluate pixel anode response by connecting several selected pixel anode nodes to the I/O pads. A ramp signal of 2 V to 1 V is input. The pixel is configured in a global shutter mode (pixels are addressed during the reset). The measured input ramp signal and OLED anode voltage output is plotted in Figure 3-40. There are eleven V_{DATA} range from 0.7 V to 1.7 V with 0.1 V step. The pulse width is modulated with varying V_{DATA}.


V_Ramp (input)
V_Ramp
V_Diode
V_DATA=0.7V
V_DATA=0.8V
V_DATA=0.9V
V_DATA=1V
V_DATA=1.1V
time(s)
×10^-3

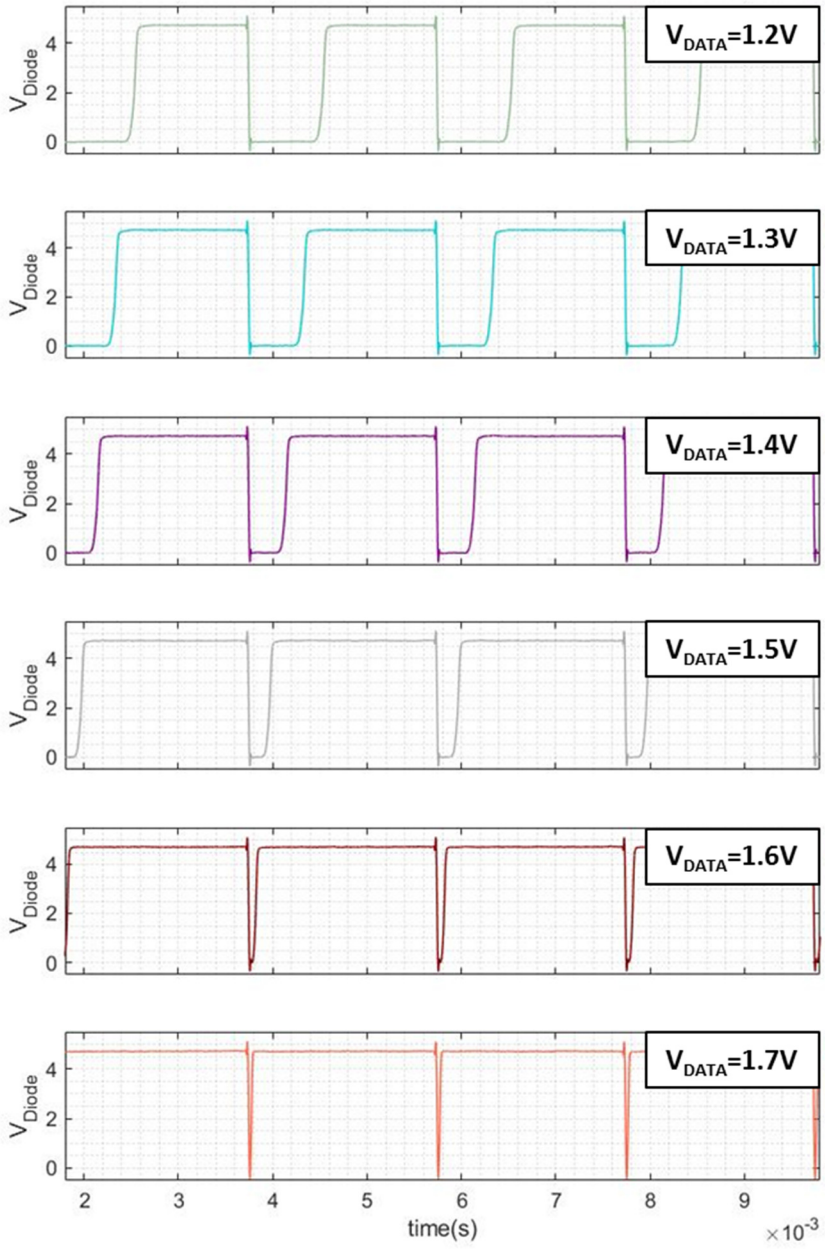


Figure 3-40 Measured Ramp signal and anode output response, V_{DATA} input as 0.7 V to 1.7 V with 0.1 V step.

3.6.3.3 PWM linearity

As it is illustrated in section 3.5.2.3, the Ramp switch point voltage correlates to the input V_{DATA} linearly. By varying the Ramp voltage in a certain shape, the pulse width can be modulated linearly or exponentially (for Gamma correction). In terms of linearity, a similar experiment is performed with varying V_{DATA}. The input Ramp signal is a linear 2 V to 1 V down-going signal as shown in Figure 3-40. The V_{DATA} is input between 0.7 and 1.7 V with a voltage step of 0.05 V. However, the switch point voltage is marked as the V_{Anode} crosses the half of V_{DD} (2.4 V) rather than the half of I_{Anode}. The reason is the difficulty to measure individual pixel current. The extracted switch point voltage is shown in Figure 3-41 against a linear fit and the residual error. The linear fit to V_{DATA} has the following parameters,

$$V_{Ramp\ switch} = 0.976\ V_{DATA} + 251.2\ mV \qquad \textbf{Equation 3-14}$$

The 251.2 mV correlates to the bias current in Equation 3-13. The higher is the I_{bias}, the higher is the value of the intercept point. The slope is less than one according to Equation 3-13 (more than one due to the charge injection effect). Two assumptions in the equation which can be invalid could explain. First, the switching point is referring to the half V_{Anode} rather than the half I_{Anode}, which is causing an extra V_{DATA} dependency on the switching point voltage. Second, the >1 slope, indicated in Equation 3-4, is derived under the assumption of fast falling rate that half of the charge is injected to V_C. If the switch is turned off slowly, most of channel charge is returned to the source terminal (V_{DATA}). The charge injection could be less in reality, but the effect of clock feedthrough should remain the same.

Moreover, the linear fit error, as demonstrated in Figure 3-41, is less than 6 mV in general. Although it seems like poly-nominal shape between 1.25 V and 1.65 V, it is quite randomly distributed over the other voltages and as a whole. The charge injection and clock feedthrough possibly introduce the nonlinearity error at V_C storage point. The higher order nonlinearity of the charge injection could affect the switch point voltage.

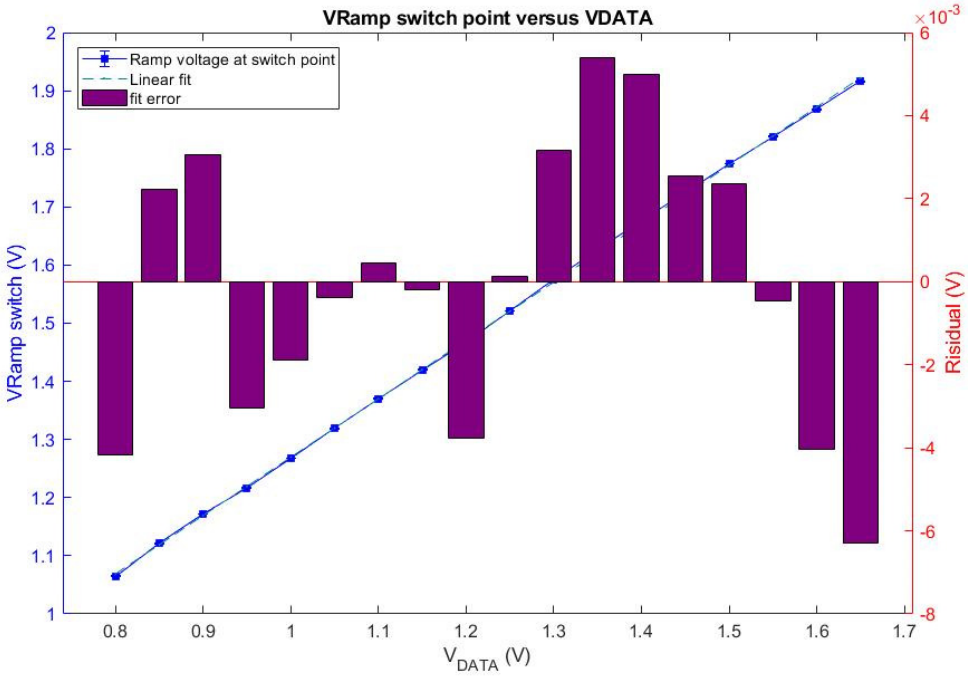


Figure 3-41 the relationship of Ramp switch voltage to V_{DATA} voltage (left axis) and linear fit error (right axis); the Ramp switch voltage error bar shows the measurement repeatability error

3.6.3.4 Non-uniformity across the array

As it is shown in Figure 3-37, the pixel layout is arranged in a 2 × 2 (quad) format to share n-well and achieving a small pixel pitch. Thus, it is anticipated that there is a certain level of mismatch between the 2 × 2 pixels. Due to the limitation of I/O ports, only six pixels' anode nodes are connected for electrical measurements. There are four pads dedicated to red marker pixel (North-western) in the 2 × 2 pixels, labelling as 1, 3, 11 and 27. Pixel 1 and 11 are meant to evaluate the RC delay effect on the Ramp signal, as they share the same row-wise Ramp signal. Pixel 1 and 27 are meant to evaluate the mismatch of the Ramp signal between different rows. Moreover, pixel 38 and 48 are selected to measure the mismatch between pixels in the blue marker (South-eastern) of the 2 × 2 structure. Pixel 38 is at the beginning of the row, and pixel 48 is at the end of the row.

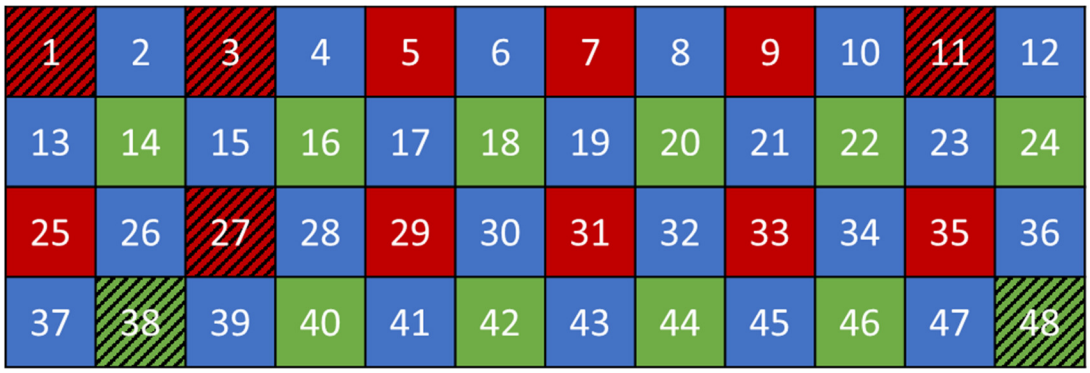


Figure 3-42 2×2 arrangement in the 4×12 array, the patterned fill cells indicate the location of the pixels that are connected to external IOs.

The scatter plot of the ramp switch point voltage is shown in Figure 3-43. It is obvious that the data points are split into two groups. Pixels that located in the red markers (no. 1, 3, 11, 27) have similar switch point values. The pixels that located in the green markers (no. 38, 48) have different switch point voltages which deviate from the red markers. It is in accordance with the conjecture that the mismatch between pixels located in the different location of each 2 × 2 structure.

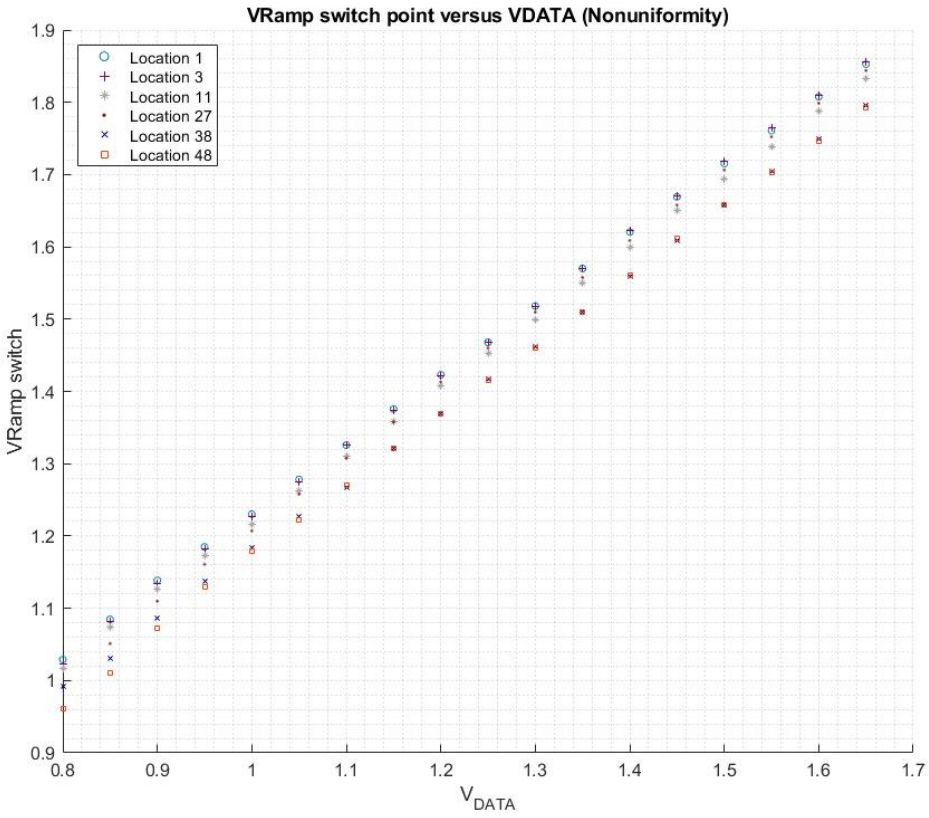


Figure 3-43 the scatter of the ramp switch point versus V_{DATA}

Figure 3-44 illustrates the linear fit and the resulting residual error for switch point versus V_{DATA} fit of pixel 1, 3, 11 and 27. The extracted linear regression equation is,

$$V_{Ramp\ switch} = 0.9734\ V_{DATA} + 246.4\ mV \qquad \textbf{Equation 3-15}$$

Figure 3-45 shows the linear fit and error for pixel 38 and 48. The following equation describes the linear fit,

$$V_{Ramp\ switch} = 0.9611\ V_{DATA} + 213.5\ mV \qquad \textbf{Equation 3-16}$$

There are mainly two transistors mismatch that is causing the non-uniformity variation. The first primary source of mismatch is from the switch transistor MN2. Different V_{TH} and mobility lead to a different switch point voltage from Equation 3-12. The mismatch of MN2 is worse if the geometric layout is not in a common-centroid manner [173]. This explains the mismatch of the pixels located in the different location of the 2 × 2 structure is worse than the pixels locating far from each other. The second source is the mismatch of Write transistor MN1. The MN1 is critical for the charge injection at

the storage node V_C. Moreover, it is designed to be minimum pitch (0.5μm × 0.5μm) which could result in a poorer matching performance.

In general, the most substantial error is less than 0.035 V for the voltage range 0.8 V to 1.65 V. If the valid input range reduces to 0.9 V to 1.65V, the non-uniformity error is reduced to less than 0.02V. Although there is only six pixels measured, the results is in agreement with the 2.4% 3σ range.

Regarding a 2V peak-to-peak input ramp, the non-uniformity variation can be less than 2% of the overall pulse-width.

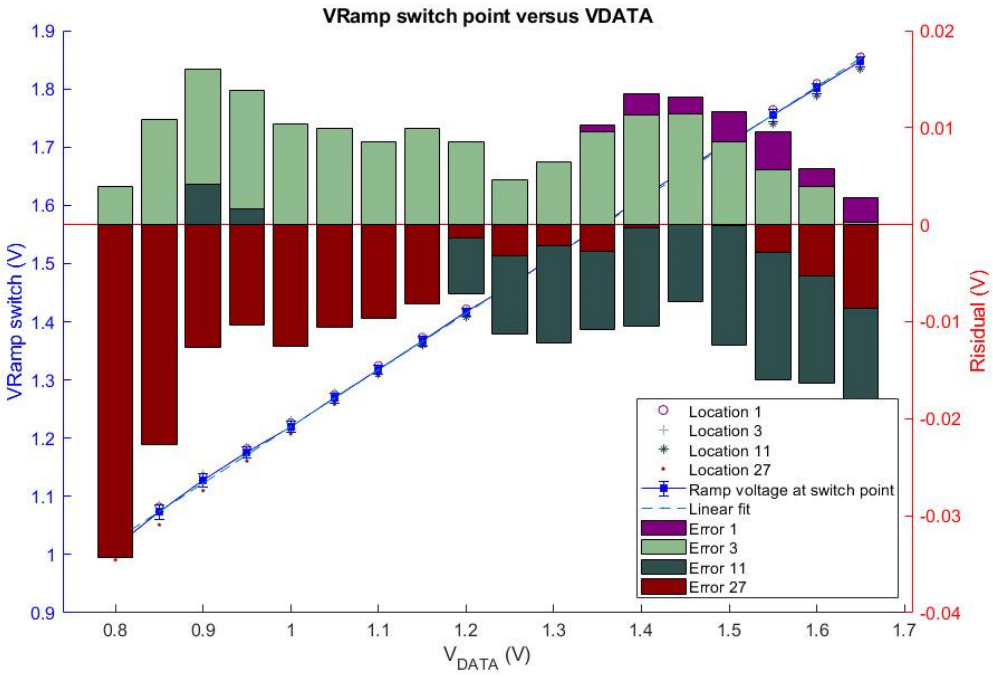


Figure 3-44 Linear fit and error residuals for the pixels 1, 3, 11 and 27

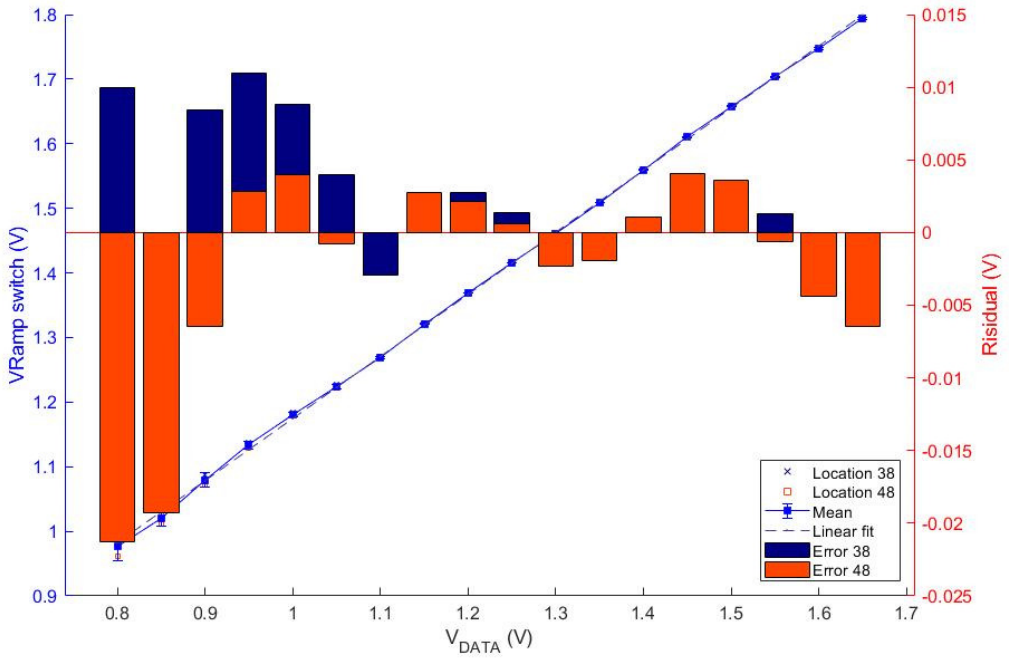


Figure 3-45 Linear fit and error residuals for the pixels 38 and 48

3.7 Summary and Conclusions

This chapter details several pixel circuit designs for tandem structure OLED microdisplays, including a conventional 2T SF circuit; an enhancement of the 2T SF circuit; and a novel analogue PWM circuit. All of them are implemented in test pixel arrays to drive tandem-structure OLED.

For the 2T SF pixel with annular MOSFET switch, lower leakage is demonstrated in the flicker measurement. It allows input DATA voltage to be lower than the threshold voltage, improving the available input voltage range. However, the electrical measurement through connecting to I/O pads introduces secondary effects to the measured anode response. Chapter 4 presents the optical measurements of the pixels that can be compared with the simulations.

The test array pixel is a proof of the concept that a TOLED microdisplay pixel using analogue PWM approach can be minimised in pitch to 5 × 5 μm^2 subpixel. The results from this test pixel are tabulated against the Blalock PWM in Table 3-4. With much less transistor, the novel analogue PWM pixel occupies only 17.4% area equivalent to the Black pixel. Besides, the pixel power consumption is less without any bias current required. Moreover, the PWM pixel is in line with the Blalock pixel in terms of simulated non-uniformity.

Table 3-4 A comparison table of the analogue PWM pixel in this work with the Blalock PWM pixel

Author (Reference)	This work	Blalock ([6])
Sub-pixel pitch	5 × 5 μm^2	12 × 12 μm^{2*}
Transistor counts (including MOS capacitors)	6 T	19 T
Bias current	None	12 nA
CMOS process	STMicroelectronics 0.13μm	Agilent Technologies 0.35μm
Monte-Carlo simulated pulse-width 3σ variation	2.4 %	2.3 %
Measured non-linearity	Less than 0.6 %	N/A
Measured non-uniformity[30]	Less than 2 %[31]	N/A

*monochrome

The new analogue PWM pixel pitch is comparable with the state-of-the-art pixels, mentioned in Table 3-1. However, it is with more functionality in-pixel. The chapter demonstrated that the pixel design performs well in test structure scale to drive the novel tandem structure OLED. It can be scaled to a larger array in terms of performance and pixel pitch.

[30] Only for the 4 × 12 test array and only pixels in the same location of the 2 × 2 quad structure
[31] For reduced voltage range of 0.9 V to 1.6 V with a 2 V to 1 V ramp

4 Characterisation of OLED microdisplays using advance CMOS SPAD sensors

4.1 Introduction

This chapter explores the application of CMOS single-photon avalanche diode (SPAD) sensors for characterisation of microdisplays. Based on the OLED microdisplay arrays presented in chapter 3, we demonstrate the use of CMOS SPAD sensor to perform optical measurements at a very high frame rate, a very low light level and over a very wide dynamic range of luminance. These characteristics offer a huge potential to reveal hitherto obscure details of the optical characteristics of individual and groups of OLED pixels.

The chapter is split into three parts. The first provides an overview of instruments employed for display measurements including single-point sensor and image sensors. Published metrology setup and the sensors are also reviewed. The second presents a detailed analysis of the application of a single-point SPAD sensor in photon counting mode for a fast transient measurement of OLED pixel flicker. The third details a SPAD image sensor operated in QIS (Quanta Image Sensor) mode for high dynamic range measurements and fast transient measurements for OLED microdisplay pixel.

4.2 Display/Microdisplay measurements overview

To specify and compare electronic displays, their optical performance needs to be measured and quantified in absolute units. The optical measurements/characterisation are more challenge than electric measurement. The display quality highly depends on the environment of the observer and the display content. External factors are influential to the measured parameters. Some display measurement might be trivial to the observers. On the other hand, some insignificant differences from the display measurement could be evident to the observers.

In order to minimise the potential measurement error, appropriate measurement setup/instrument according to the requirements are essential. Electronic display technologies have evolved from Cathode Ray Tube (CRT) to LCD, Plasma panel display (PDP), and more recently OLED and micro-LED (μLED). The display measurement setup also advances, and specific measurement tasks are designed for various technologies.

More details of optical characterisation of direct-view and projection based displays can be found in the Handbook for Visual Display Technology [174] and the Information Display Measurements Standard produced by the International Committee for Display Metrology [175]. The research of display

measurements includes photometry, test patterns and measurement devices etc. In this chapter, we will focus on the measurement devices employed for microdisplay measurements.

There has been a significant effort in developing microdisplays for augmented reality (AR) and virtual reality (VR) head-mounted displays (HMD). The demand for measuring the photometric and colourimetric properties of AR/VR devices are escalating.

4.2.1 Optical experiment setup

Conventional display measurements are usually designed to measure the light output from the real images (projection or display panel). However, AR/VR devices are meant to create a virtual image onto a human eye. As shown in Figure 4-1 (a) [176, 177], the optical structure of VR devices are designed to be compact to be worn on the head. A lens is placed in a short distance between the display and the human eye. A virtual image is created as light rays enter the human eye and focus on the focal plane (retina) through the eye lens. Based on the pupil diameter and the focal distance, the eye position may require to move to cover the full virtual image. Therefore, Tsurutani et al. from Japan Electronics and Information Technology Industries Association developed an experimental setup as shown in Figure 4-1 (b) [176]. Depending on the lens pupil size of the image sensor, it is necessary to move the sensor to cover the full field of view (FOV).

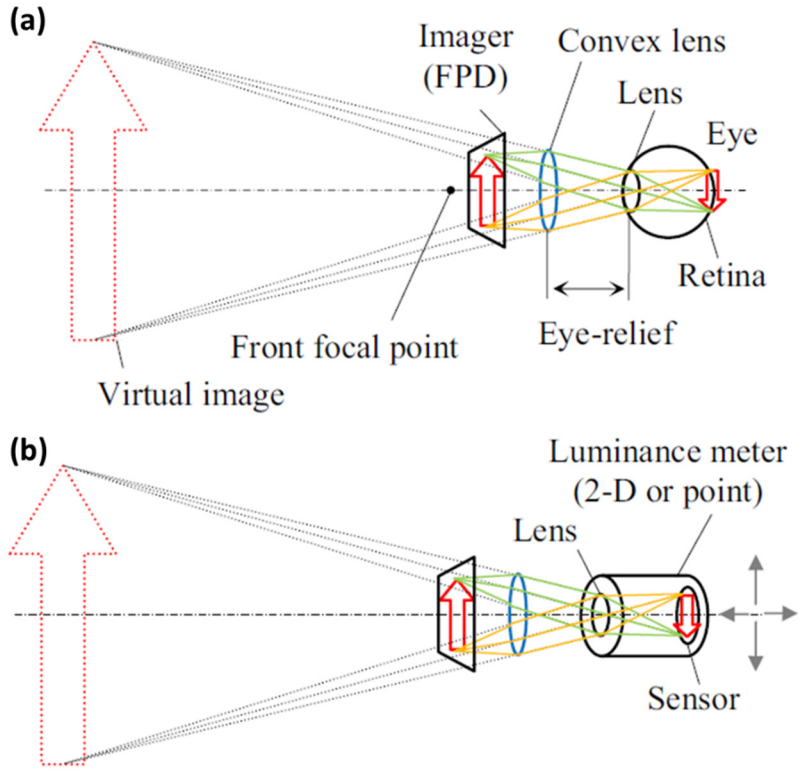


Figure 4-1 (a) Principle of virtual optics for microdisplays (b) Example measurement setup for microdisplays (source [176, 177])

4.2.2 Luminance sensors

There are several different types of sensors applied as luminance measurement devices for display measurements.

4.2.2.1 Single spot detectors

Spot detectors are one of the typical types of luminance meter. The block diagram of a spot detector is shown in Figure 4-2. The input light is filtered before reaching the detector. The optical filters can be either spectral filters which adjust the spectral sensitivity and neutral density filters which modifies the intensity of the all wavelength to increase the dynamic range of the dedicated detector. The spectral sensitivities depend on electronic detectors like photodiodes. The source of errors is photon shot noise, detector measurement error and the noise from the analogue digital conversion.

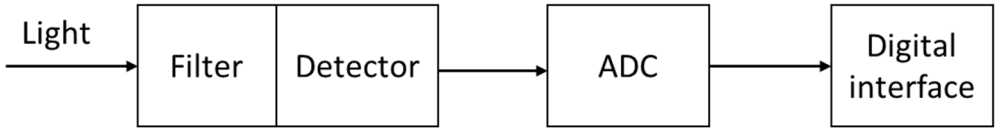


Figure 4-2 Block diagram of a typical luminance meter

4.2.2.2 Calibrated camera

Detectors with camera systems are superior for measurements that required a wide field of view, such as non-uniformity, motion blur and cross-talk etc. They are normally equipped with a CMOS or CCD sensor with millions of pixels. Figure 4-3 shows the stereotypical optical setup realised by an array of detector element (i.e. cameras). The incident light is split spatially into each detector element. The use of calibrated cameras for luminance meters are growing with the rapid development of CMOS technology. However, the SNR, dynamic range and sampling rate are comparably worse than single point sensors.

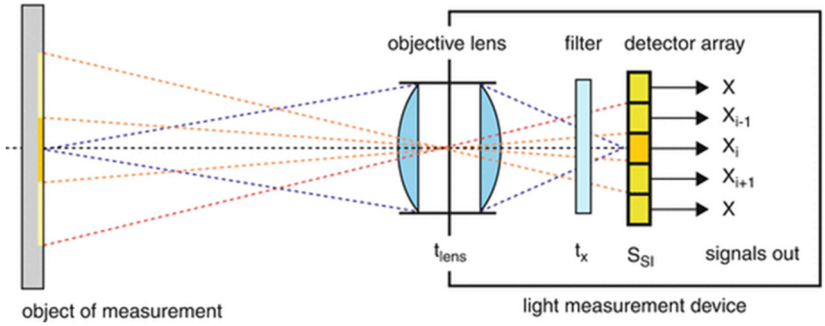


Figure 4-3 Block diagram of light measurement devices which employ imaging array (cameras) (source: [178])

4.2.2.3 Spectrum/line detector

Line sensors are usually employed for spectrometer setup that measures light over a specific portion of the spectrum. An example block diagram for a configuration of a SPAD sensor as a spectrometer based FLIM system is shown in Figure 4-4. The fluorescent emission is spread by a grating into a spectrum. Spectrometers are used widely in spectroscopy for measuring wavelengths and intensities. It can also be used for colour spectrum measurement for display metrology.

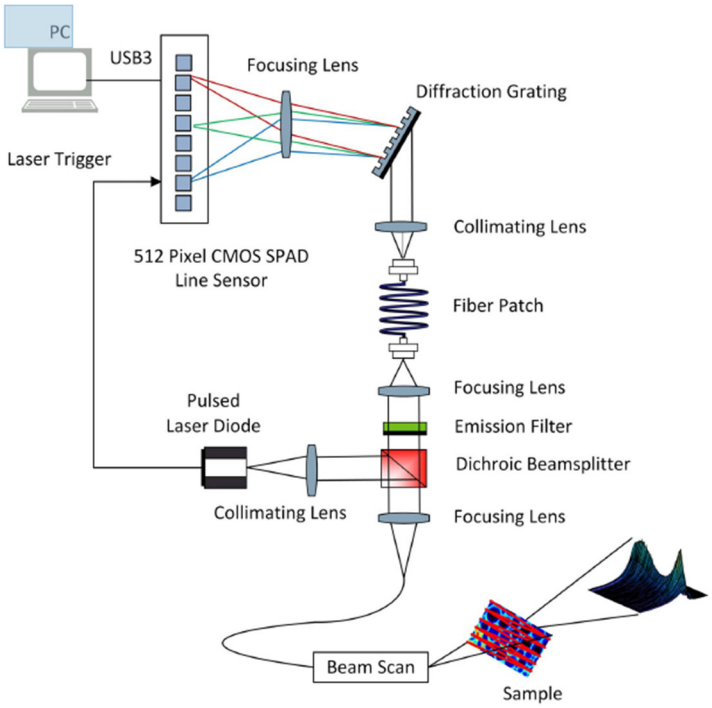


Figure 4-4 Example optical setup of a SPAD line sensor as a spectrometer based FLIM system (Source:[179])

4.3 Single photon detectors for display measurement

Photon counting offers advantages of high sensitivity for extremely low optical power signal and high accuracy with a low noise level. Conventional photon counting technology such as photomultiplier tube [180-182] and streak camera [183] have been employed for characterization of both LCD and OLED displays. The photon counting technology is beneficial for characterizing high-performance displays that can present low contrast detail in the images [182] and for transient temporal behaviour such as photoluminescent (PL) lifetime decay of Alq_3-based OLED [183]. High dynamic range and fast switching time are key characteristics for display/microdisplay systems [174]. The prior indicates the grey scale modulation of a display. Due to the brightness perception of human eyes, sensitivity to relative differences between darker conditions is greater than brighter ones [184]. It is worth to reveal

the low contrast subtle detail in the display images. The latter is essential for image quality of moving content like animation and movies. The switching transition time (rising[32] and falling[33]) for LCD [185] are typical ~millisecond and for OLED can be as low as nanosecond [59, 183]

4.3.1 Historical photon counting detector for display measurements

4.3.1.1 Photomultiplier tube (PMT)

A photomultiplier tube is built based on the photoelectric effect discovered by Hertz in 1887 [186]. It is composed of a photocathode and secondary emission multipliers. A photon is converted to electron through the highly sensitive photocathode. The secondary emission multipliers (dynodes) amplifies the photoelectron gain to magnify the photon signal. The first reported PMT with a dynode was developed by Austin et al. [187] Figure 4-5 shows the construction diagram of a photomultiplier tube. When light detected by a PMT, an output signal is processed through the following:

a) Light input through the faceplate
b) Electrons are excited in the photocathode with photoelectrons emitted to the vacuum chamber
c) The photoelectrons are accelerated and focused by focusing electrode and multiplied by the dynodes
d) The multiplied secondary electrons emitted from the last dynode and collected by the anode

More information about the basic principle and operation of PMT are available in [188].

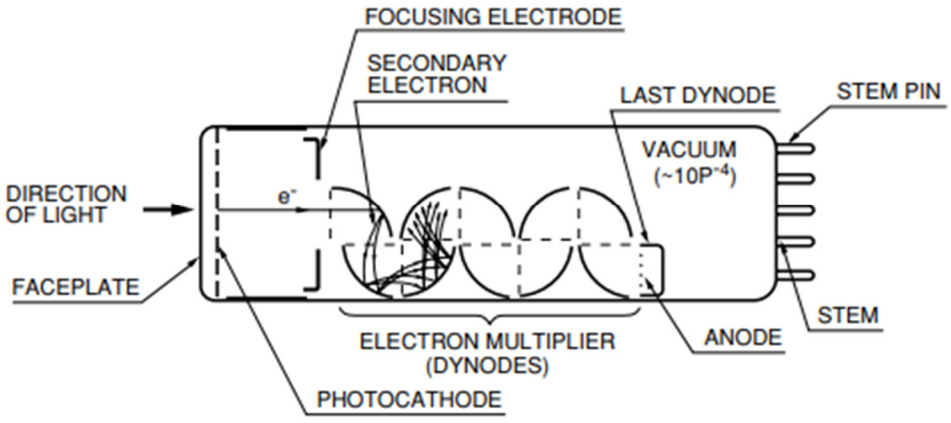


Figure 4-5 Schematic diagram of a photomultiplier tube [188]

The output from a PMT can be processed electrically via different operation modes. Figure 4-6 shows the typical block diagram for using PMT in: DC measurement, AC measurement and photon counting

[32] Transition time from 10% to 90% of maximum luminance
[33] Transition time from 90% to 10% of maximum luminance

modes. The DC method processes the PMT output with an amplifier and a low pass filter. It is able to measure a relatively high light levels. However, inevitable readout noise (amplifier, ADC) could affect accuracy. The AC method filters the DC component and produces a signal to describe the amplitude and the frequency of the measured signal. The photon counting mode converts detected photons into pulses. Photon counting method is the most commonly used which takes the advantages of the high sensitivity of PMT to photon level. It is capable of detecting low light level with very low noise.

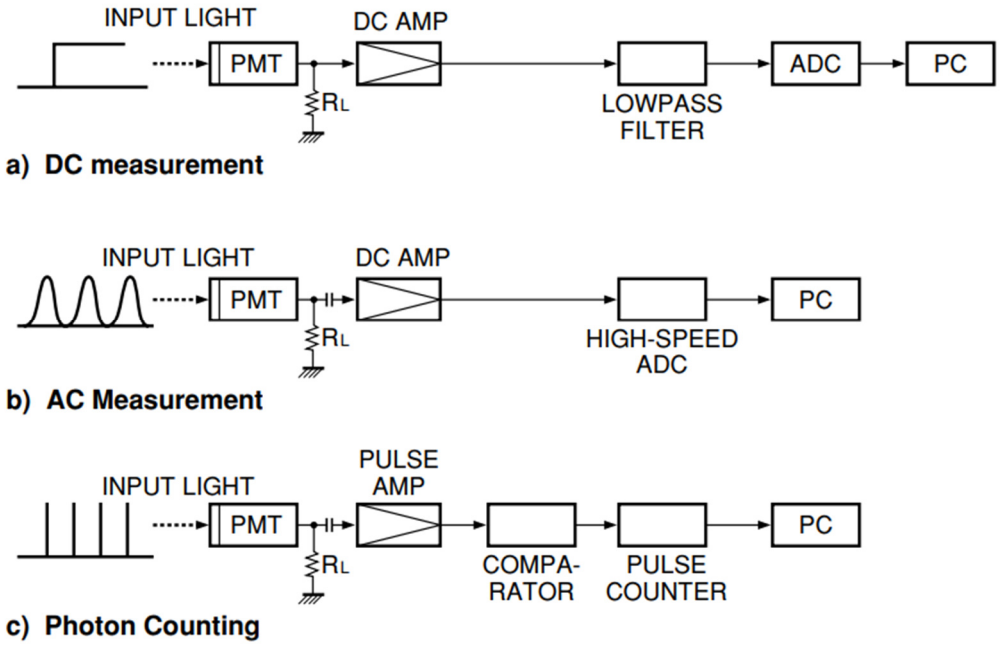


Figure 4-6 Operation modes using PMT (a) DC measurement (b) AC measurement (c) Photon counting [189]

In [180-182], Fatadin et al. from NPL (National Physical Laboratory) have applied a PMT based spectroradiometer system for display characterisation. The PMT configured in photon counting mode is advantageous to other optical measurement instruments for its high accuracy in photon counting mode. The system can cover a dynamic range of photon flux level from 10^1 – 10^7 photon counts per second. It is suitable for measurement of dim screens and small spot measurements. The NPL microscope setup with a stray-light-elimination tube (SLET) is capable of adjusting the diameter of the measurement spot from 30 mm to 100 μm. Multiple wavelength measurements range from 380 nm to 780nm with an error less than 0.05 nm.

As shown in Figure 4-6 (c), each photon arrived in the PMT is converted into an amplified pulse. A comparator with an appropriate threshold level is employed to filter the noise from signal pulses. The signal-to-noise ratio (SNR) is defined as the ratio between the mean signal photon count rate to the variation of the signal and noise count rate.

$$SNR = \frac{N_S\sqrt{T}}{\sqrt{N_S + 2(N_B + N_D)}}, \qquad \textbf{Equation 4-1}$$

Where N_S is the signal count rate from the incident light; N_B is the signal count rate from background light; N_D is the signal count rate from dark current; T is the measurement time.

Depends on different measurement setup, the PMT measurement is usually taken twice at a time. One is with the incident signal. Another is without any incident light, only measures the background and dark count rate. The signal count rate is a background subtracted value. In an ideal condition, without any noise count from background and dark current, the incident photon count rate follows a Poisson distribution. Its expected value equals the variance. The SNR becomes

$$SNR = \sqrt{N_S T}, \qquad \textbf{Equation 4-2}$$

Both the signal level (N_S) and noise level ($N_B + N_D$) increase with supply voltage. Usually, the supply voltage is a trade-off between the optimum gain and good SNR.

The PMT allows a good level of linearity with photon counting over a wide dynamic range. The minimum count rate is associated with the dark current pulse (assumed background level negligible). The maximum limit is relating to the time interval between count pulses. When a photon is received by the PMT, there is a dead time (usually +10 nanosecond) associated the photon pulse. If more than one photon is received during the pulse, the count pulses will overlap, count error is induced via pulse overlapping. A typical PMT configured in photon counting mode has a non-extendable (non-paralyzable)[34] style dead time which the second photon will increase the analogue voltage of the pulse height instead of extending the pulse width. If two photon counts arrived during the same dead time, only one pulse is recorded. During the counting period T, we assumed each detected photon generates a dead time of τ. For the true count rate of m, the detector records k counts in T. Therefore, during the dead time period, $mk\tau$ counts are lost. The compensated counts are [190],

$$mT = k + mk\tau, \qquad \textbf{Equation 4-3}$$

Compared to the conventional photodiode, the PMT is advantageous for

[34] In the extendable (paralyzable) case, the arrival of a second event during the time period extends this period by adding on its dead time; In the non-extendable (non-paralyzable) case, the element (e.g. PMT) is insensitive during the dead time period. The second event arrival is ignored, and the element is active again after a time τ.

a) Single photon sensitivity
b) Low readout noise and high SNR
c) Fast response that allows high-speed measurement

However, there are some inherent drawbacks mean it has not become a popular tool for display measurements,

a) High supply voltage required (~kV)
b) Cooling system is required
c) Extra external tools such as pulse counter, TDC, histogram hardware are required

4.3.1.2 Streak Camera

Apart from PMT, streak cameras are another type of detectors that are capable of single photon counting. Figure 4-7 shows the operating principle of the streak camera. The incident light is filtered through a slit to form a one-dimensional array in horizontal. The four incident light pulses, which vary slightly in both temporal and spatial, are converted into a number of electrons. The number of electrons correlated to the intensity of the light pulses. As these electrons are accelerated to pass through a pair of sweep electrode, a sweep voltage is applied. So the electrons are deflected in slightly different angles in the vertical direction. Thus, the incident photons, from different horizontal locations and time, will be projected to a different location on the phosphor screen. In this example, the earliest arrived photons are placed in the uppermost position and the latter ones are placed in sequential order from top to bottom. Besides, the brightness of the phosphor images is proportional to the intensity of the incident light pulses. A high-resolution camera is used to record the phosphor images.

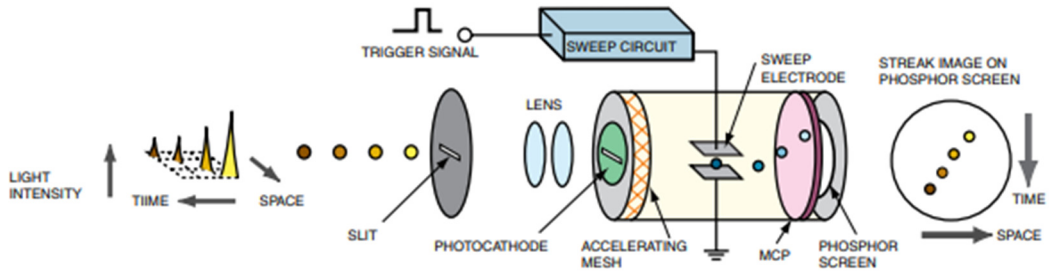


Figure 4-7 Operation of the streak camera [191]

One way to configure the streak camera is to convert the spatial axis to the wavelength axis through optics. It enables a time-resolved spectroscopy measurement to measure changes in light over time and wavelength. Excellent temporal resolution as low as 0.2 ps (correspond to 0.06 mm in location) is achieved. The streak camera covers a wide spectrum band from X-rays to near infrared rays. As there

is also an MCP stage (Micro Channel Plate)[35] before the electrons hitting the phosphor screen, the amplification achieves a high sensitivity up to single photoelectron.

Murata et al. have applied a streak camera for time-resolved transient photoluminescence (TRPL) measurement to evaluate the degradation phenomena of OLEDs [183]. The photoluminescence (PL) from degraded OLED samples exhibits an exponential decay which can be fit by mono-exponential or bi-exponential decay. A bi-exponential decay can be described by,

$$PL(t) = A_1 \exp\left(-\frac{t}{\tau_1}\right) + A_2 \exp\left(-\frac{t}{\tau_2}\right), \qquad \textbf{Equation 4-4}$$

where A_1, A_2 are the relative contribution from each exponential term exhibiting lifetimes of τ_1, τ_2.

Figure 4-8 shows an example of the PL decay comparison between the undegraded and degraded OLED. The PL decay of undegraded OLED can be fit by a mono-exponential decay with a τ of 14.1 ns. On the other hand, the degraded OLED exhibits a bi-exponential behaviour with τ_1=14.1 ns and τ_2=6.9ns. The degraded OLED shows an extra shorter lifetime decay constant.

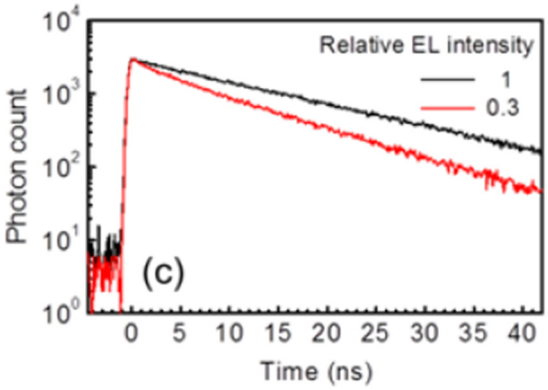


Figure 4-8 PL decay profiles of Alq_3-based OLED (black: PL decay without degradation; red: PL decay with degradation to 0.3 EL intensity) [183]

The streak camera is beneficial for photon-sparse physics measurement and picosecond time-resolution measurements. However, its requirement of complicated optical setup and the cost curb its potential for application in display measurements.

[35] The MCP is an electron multiplier composed of thin glass capillaries (channels).

4.4 CMOS SPAD

The development of single photon avalanche diode (SPAD) has led to great advances since the research of p-n junctions at Shockley Laboratory in the early 1960s. The first avalanche photodiodes (APD) that employed a guard ring structure by means of a low doped n-type implant surrounding an n^+ to p-substrate junction was introduced by Goetzberger et al.[192] It becomes one of the most popular SPAD structures to date. In the late 1960s and 1970s, Haitz [193], McIntyre [194] and Webb [195] have made contributions to study the avalanche photodiodes (APD) characteristics including noise mechanisms, afterpulsing etc. It is worth to indicate that SPAD is a particular type of APD device with special designed bias and readout circuit. In the 1980s, Cova [196] established a SPAD based picosecond resolution photon counting device as a replacement for bulky and expensive PMTs. In parallel to the work of Cova, McIntyre [197] have also applied their previous developed APDs as SPAD devices. SPAD devices started to gain attention for its single photon counting sensitivity.

To date, SPADs have been designed and fabricated in a range of technologies, including InGaAs-InP [198], GaN [199]. However, the aforementioned SPAD devices are all implemented in customed CMOS processes instead of standard CMOS. This prevents SPAD devices from developing the integration of large scale detector arrays and processing electronics. This is changed in 2003. Rochas et al. [60] developed the first SPAD device in a standard 0.8 μm CMOS process. This spurred a new era of research of highly integrated SPAD sensors for a variety of photon counting and time-resolved applications, including multi-million European projects such as MegaFrame [200], POLIS [201].

4.4.1 SPAD operation principles

There are three operation regions for a reverse biased photodiode: photoconductive (photodiode), avalanche (APD) and Geiger (SPAD) as shown in Figure 4-9. They describe the behaviour of a p-n junction diode with different reverse bias.

In mainstream image sensors (such as CCD, CMOS cameras), photodiodes are biased to a relatively low voltage in the photoconductive region. The gain is approximately 1 electron per incident photon. The readout current is linear to the intensity of the incident light.

As the reverse bias voltage increases to close to the photodiode's breakdown voltage V_{BD}, the junction is biased in the avalanche region. The avalanche current shows an amplified incident light intensity. The photoelectron gain is higher in this mode. The multiplication (gain) is controlled by the reverse bias. The gain is usually configured to around 10~100 so that the signal to noise ratio is not affected by the increased sensitivity.

For a reverse bias above V_{BD}, the photodiode is then operating in Geiger mode. The high electric field causes a large self-sustaining avalanche whenever a photon arrives. The high avalanche current causes the photodiode bias to reduce to less than V_{BD}. The photodiode is not sensitive until the bias voltage is recharged.

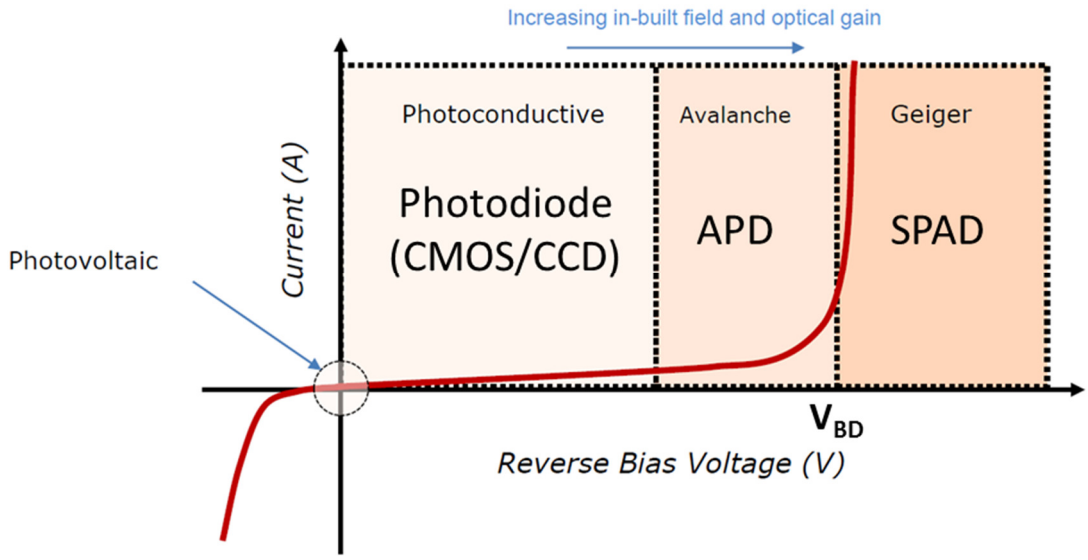


Figure 4-9 Gain versus reverse bias, the operation of different bias regions are labelled

The SPAD sensitivity (probability of avalanche occurring) is controlled by the excess bias V_{EB} above V_{BD} applied to the p-n junction. Increases the V_{EB} will increase the ionisation rate. As shown in Figure 4-10, there are five stages of the avalanche processes. Seeding: the ionisation of a photon will produce a free charge into the depletion region; Built-up: the local current density increases rapidly and the seeded area voltage will decrease to V_{BD}; Spreading: the entire diode starts the avalanche, the diode current increases as bias decrease; Quenching: the avalanche stops as the diode voltage being reduced to V_{BD}. The SPAD is not sensitive at this stage; Recharging: a passive or active quench circuit begins to restore the excess bias across the diode.

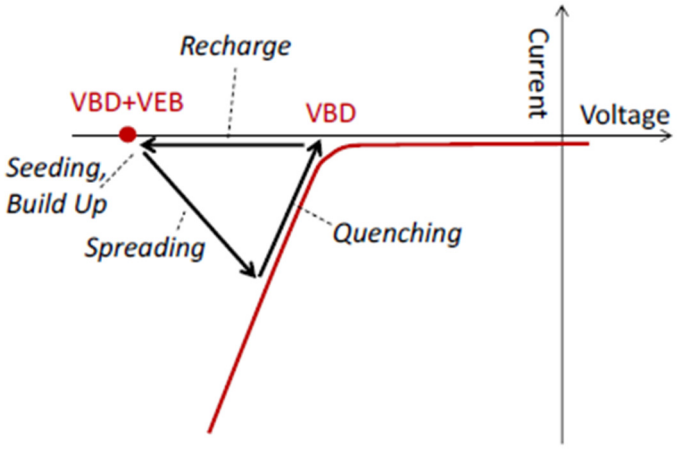


Figure 4-10 SPAD operation I-V plot in five stages

Figure 4-11 (a) shows a typical passive quench SPAD pixel frontend. The resistor recharges the diode to $V_{EB}+V_{BD}$ to restore the photo-sensitivity. The SPAD anode is then buffered by a CMOS circuit (an inverter is shown here). In Figure 4-11 (b), the avalanche produces a voltage spike which is then converted to a pulse output signal. The rising edge of the voltage spike records the arrival of a single photon with a temporal resolution of 10 to 100 picosecond [202]. The intensity of the incident light can be measured by counting the output pulses.

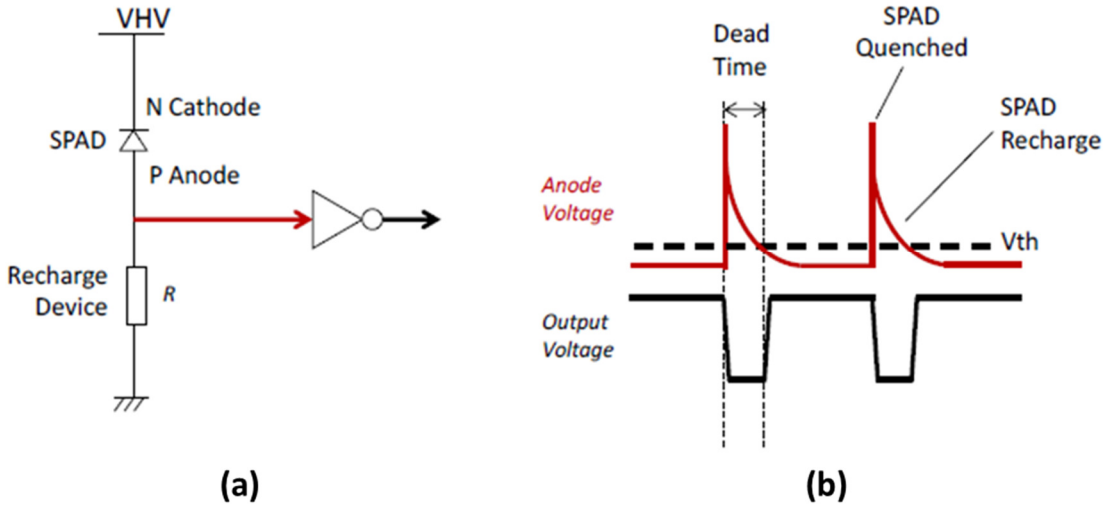


Figure 4-11 (a) schematic of a typical frontend of a SPAD pixel; (b) Waveforms of quench and recharge behaviour of the SPAD circuit.

4.4.2 SPAD Performance Parameters

The performance parameters of SPADs include photon detection probability (PDP), dark count rate (DCR), jitter (temporal response) afterpulsing and crosstalk.

PDP is a measure of the SPAD device sensitivity over the spectra of the incident light. It is related to the SPAD intrinsic quantum efficiency (IQE) and the SPAD avalanche triggering probability. The avalanche probability is determined by the excess bias voltage. Higher excess bias increases the avalanche triggering probability. However, higher V_{EB} also increases the noise level. There is a trade-off between achieving a high avalanche triggering probability and SNR [203, 204] for setting V_{EB}. The photon detection efficiency (PDE)[36] is the PDP multiplied by the sensor fill factor (FF). Figure 4-12 shows a diagram of PDP versus wavelength for a typical SPAD device implemented in the 130 nm CMOS technology by STMicroelectronics (STM). It is worth noting that the SPAD devices employed in the following sections share the same structure and same CMOS process as [205].

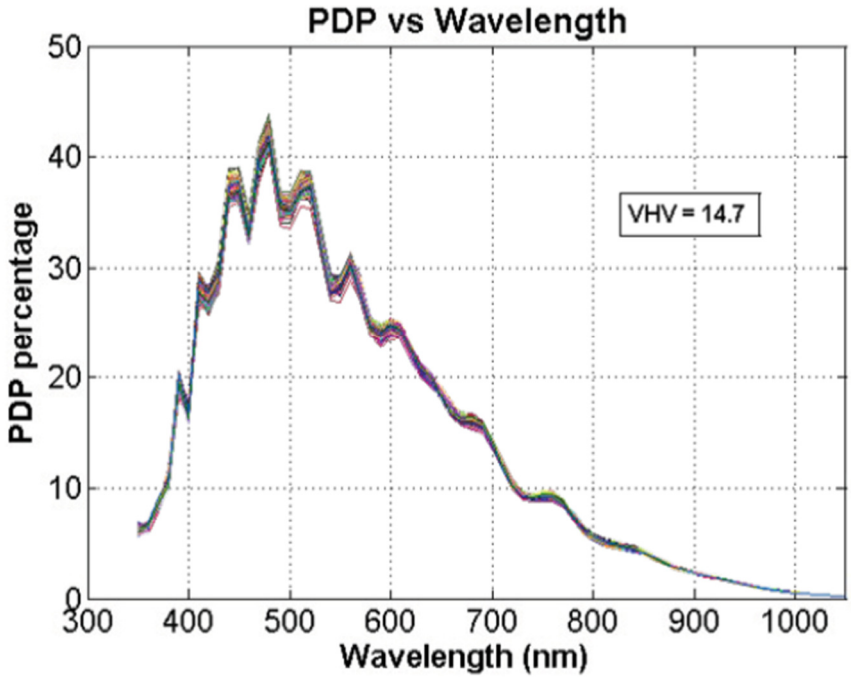


Figure 4-12 PDP versus wavelength for a typical SPAD in the 130 nm CMOS technology by STMicroelectronics at room temperature and 14.7V reverse bias [205]

DCR is the count rate that has no contribution from photon detections. It is generated by the thermal excited carriers, or defects in the charge traps, or from the band to band tunnelling (BTBT) [206]. The thermal generation is determined by the temperature. And BTBT is dependent on the electric field of the p-n junction. Therefore, DCR can be reduced by cooling the device or reduce the V_{EB}. The DCR

[36] PDE is also the SPAD extrinsic QE (EQE).

characteristics versus temperature and VHV (V_{BD}+V_{EB}) of the STM 130 nm SPADs are shown Figure 4-13 (a) and (b).

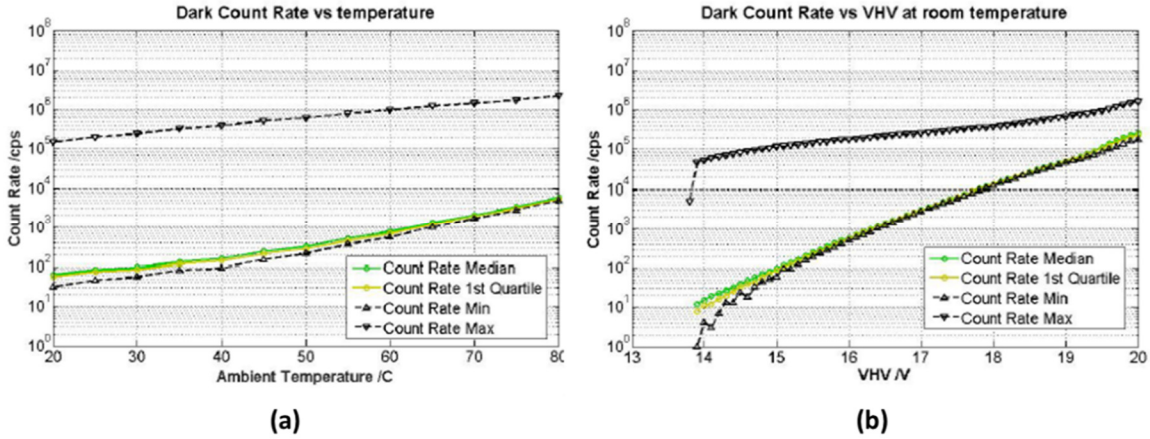


Figure 4-13 (a) DCR versus temperature (b) DCR versus VHV at room temperature. Median (green) and the 1st quartile population (yellow) are shown, the behaviour of the SPADs with minimum and maximum DCR are shown as black points with segmented lines[205]

SPAD jitter or temporal resolution is a measure of statistical variation from the moment of a photon arrival in the p-n junction to the moment of generating an output pulse. It is evaluated by the impulse response function (IRF) with respect to an infinitesimal laser pulse. The quantification value is determined by the full-width half-maximum (FWHM) of the IRF. The typical FWHM is measured to be ~100ps which is negligible for display measurements.

Afterpulsing and crosstalk are secondary performance figures for SPAD devices. The mechanism of afterpulsing is similar to DCR. It is induced by impurities and crystal defects in the junction. It can be reduced by decreasing the excess bias or in a photon-sparse condition that there is enough time between two avalanche events allowing the traps to be empty.

Optical crosstalk is usually more common than electrical crosstalk[37] in avalanche devices. An avalanche event can generate hot carriers and the latter cause a secondary photon emission [207] that detected by other pixels. However, the effect is more reported from miniature arrays that SPAD devices are close without enough spacing.

[37] Electrical crosstalk is caused by an electron-hole pair gets detected by a neighbouring device. It can be resolved by isolating the SPAD pixels with implant walls or deep trench isolation

4.5 SPAD Sensor Architectures

Thanks to the broad applications time-resolved imaging, SPAD arrays (sensors) have been developed for more than a decade and matured considerably. A variety of SPAD sensors' architectures have been proposed over the years. Based on the SPAD pixel arrangement, the existing SPAD sensors can be classified into three categories: single point sensor, line sensors and image sensors.

Line sensors are made of a one-dimensional (1-D) SPAD array of pixels with processing circuitries. Similar to the streak camera, it can be configured for spectral measurements or as line by line scanning systems for two-dimensional imaging.

An example of the state-of-the-art single point sensor and image sensor will be detailed below. Moreover, they are used for the OLED microdisplay measurements.

4.5.1 Single point sensors

As it is suggested, this group of SPAD sensors work as a single pixel performing single point measurements. Similar to a PMT operating in digital mode, the single point SPAD sensor is also known as a digital silicon photomultiplier (dSiPM). Although, there is pixel circuit integrated for each SPAD. It outputs a single channel digital pulses which combines an array of SPAD pixels. The spatial resolution is sacrificed for the purposes of large active area (with low dark count level) and multiple photon time stamping. Moreover, the SPAD pixels in dSiPM are usually with minimum circuitry to optimize pixel area and fill factor.

Single point SPAD sensors are widely used in mobile phones for proximity sensors for screen locking and camera auto-focus assistance [208]. Another popular application in biomedical research is FLIM and PET (Positron emission tomography). Several research groups have developed early demonstration of single point sensors including SPAD arrays combined by an OR tree [209], with TDC integrated on-chip [210] and multiple interleaving TDCs for improving conversion throughput [211]. Multiple interleaving TDCs are used to resolve the requirement of the TDC dead-time before a new conversion. However, different TDCs can introduce error to the measurement due to mismatch.

4.5.1.1 Dynamic range of dSiPMs

As a single point sensor used for luminance measurement, dynamic range is one of the key characteristics. Similar to photon counting mode PMTs, each photon event introduces a dead time to the detector. The dynamic range of SPAD is limited due to photon pile-up. In the case of an ideal dSiPM, where each pixel has its own counter circuitry [212], the average count rate of the array can be described by,

$$m_0(n) = N \cdot n \cdot \exp(-n \cdot \tau_d), \quad \textbf{Equation 4-5}$$

where N is the number of pixels, n is the arrival photon rate, τ_d is dead time.

Moreover, the maximum output count rate is equal to

$$\max\big(m_0(n)\big) = \frac{N}{e \cdot \tau_d} \Leftrightarrow n = \frac{1}{\tau_d} \quad \textbf{Equation 4-6}$$

The count rate is limited by the pile-up of each individual channel itself and the counting circuitry. However, individual in-pixel counter circuitry reduces the fill factor. In practice, most of the multichannel dSiPM consist of an N-to-1 combining network. Lost counts can be introduced by the pile-up of the combining network.

There are several techniques of combining the pulses which would affect the SPAD single point sensor bandwidth. As shown in Figure 4-14 (a), the conventional OR tree network cannot record additional SPAD events in different SPAD pixels if the time interval between two SPAD firing is less than the dead time. The two pulses are merged, the pulse extends a dead time from the second SPAD firing. The behaviour is similar to the pile-up in passive recharge pixels which is an extendable (paralyzable) case mentioned in section 4.3.1.1 [213]. The equation of the measured count rate and the actual count rate can be written in a similar way to a paralysable detector [214],

$$m_{OR}(n) = m_0(n) \cdot \exp(-m_0(n) \cdot \tau_d), \quad \textbf{Equation 4-7}$$

where $m_0(n)$ is the count rate input to the OR tree, $m_{OR}(n)$ is the OR tree output count rate, τ_d is the dead time.

The maximum measureable detection rate is equal to,

$$\max(m_{OR}) = \frac{1}{e \cdot \tau_d} \Leftrightarrow m_0(n) = \frac{1}{\tau_d} \quad \textbf{Equation 4-8}$$

The detection rate for dSiPMs with OR tree configuration is quite limited. It is suitable for low light applications that a large active area (high number of pixels) with low DCR is required.

In order to extend the dynamic range, additional pulse-shortening monostable circuit is adopted [215, 216]. The example circuit diagram and waveforms are shown in Figure 4-14 (b). The dead time is effectively reduced to the output pulse width of the monostable output. Equation 4-7 becomes,

$$m_{OR}(n) = m_0(n) \cdot \exp(-m_0(n) \cdot PW)\,, \qquad \textbf{Equation 4-9}$$

The dead time τ_d is replaced by shortened pulse width PW. It can achieve a maximum count rate of,

$$\max(m_{OR}) = \frac{1}{e \cdot PW_{min}} \Leftrightarrow m_0(n) = \frac{1}{PW} \qquad \textbf{Equation 4-10}$$

where PW_{min} is the minimum achievable pulse width. And the maximum actual photon arrival rate that can be measured is

The pulse widths of the monostable circuits can be designed as low as a few hundred picoseconds [217].

However, the routing of extra bias is required to configure the monostable circuit and dead time mismatch is introduced. Recent works have presented the use of toggle cells with XOR tree replacing the OR gate structure. Each transition (toggle) of the pulse train output contains the timing information of the photon events. Both edges of the toggling signal can be combined by the XOR gates without the need of pulse width shrinking. An example waveform diagram is shown in Figure 4-14 (c). There is an upper limit for this toggle with XOR tree – when two photon events are very close in time (less than a gate delay) and propagate through the same XOR gate, these events will be cancelled out and result in loss of information. The bandwidth limitation model is in a similar way of a nonparalysable detector model (as in section 4.3.1.1),

$$m_{XOR}(n) = \frac{m_0(n)}{1 + m_0(n) \cdot PW_{min}}, \qquad \textbf{Equation 4-11}$$

where PW_{min} is the minimum pulsewidth limited by the ability of the electrical signal.

The maximum count rate is

$$\max(m_{XOR}) = \frac{1}{PW_{min}}, \qquad \textbf{Equation 4-12}$$

On the other hand, the maximum $m_0(n)$ follows Equation 4-6. Thus, if $\tau_d \gg PW_{min}$, the bandwidth of XOR gate is similar to a dSiPM with individual in-pixel circuitry/counter as in Equation 4-5.

Therefore, higher throughputs are predicted for XOR-based dSiPMs compared to conventional OR-tree based by the simulation model. And it is proved by measurements in real silicon [218].

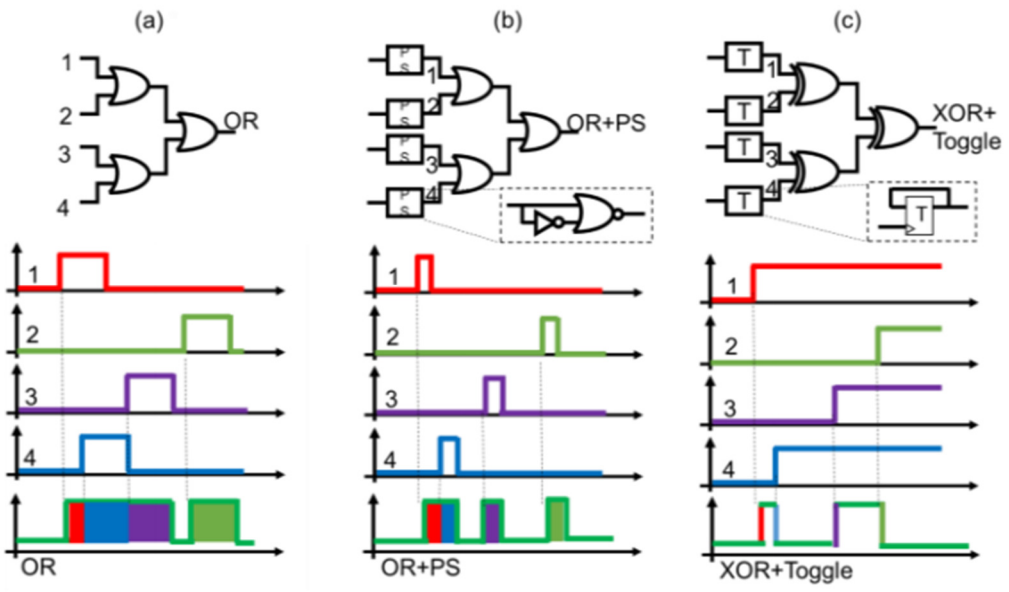


Figure 4-14 (a) OR Tree (b) OR tree with monostable pulse shaper input (c) XOR Tree with toggle flip-flop input.

If readers are interested, more information about modelling OR/XOR pulse combining techniques can be found in [213, 214, 218, 219].

4.5.1.2 FlashTDC sensor

In 2015, Dutton et al. reported a 32 × 32 dSiPM with a novel folded flash TDC architecture with a throughput of 14 GS/s and histogram on-chip in [220]. A photomicrograph of the dSiPM device, labelled as FlashTDC, is shown in Figure 4-15. The FlashTDC sensor features a 21 µm pixel pitch and 43 % filled factor. The output of each SPAD front-end is connected to a toggle flip-flop with XOR tree structure as shown in Figure 4-14 (c). The photon arrival is encoded via an asynchronous dual-data-rate manner. Moreover, a novel Multiple Event TDC (METDC) is integrated to record the timing of each individual photon up to maximum 10 Giga Sample / Second. The exposure time can be set as small as 27.78 ns to capture fast transient optical events. And a minimum readout time of 5.3 µs is required. The individual frame time is exposure time + readout time.

Similar to the photon counting mode PMT, the readout noise is negligible. The signal to noise ratio is limited by the Poisson shot noise and background noise. It can be described by Equation 2-1.

FlashTDC has been employed as a single point sensor for high dynamic range and fast transient measurements.

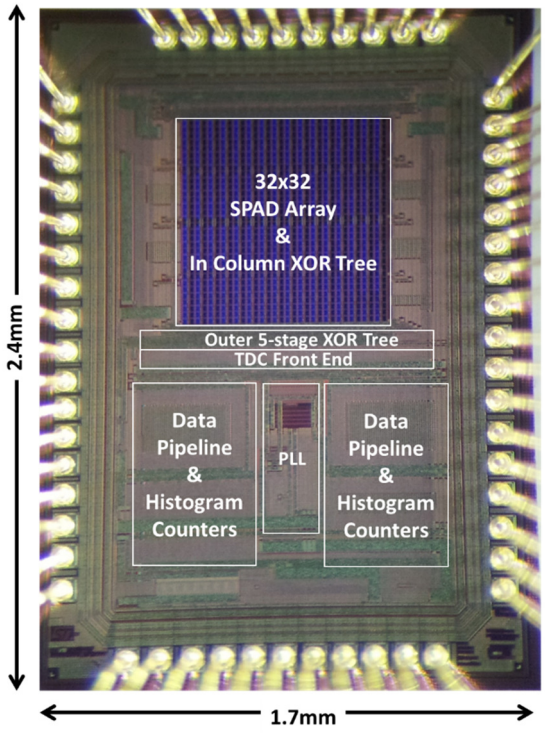


Figure 4-15 photomicrograph of the FlashTDC chip used in this work. [221]

4.5.2 Image sensors

SPAD image sensors, which are similar to CISs, contains a 2-D arrays of pixels with individual SPAD coupled to its own dedicated circuitry. In the early days, the SPAD image sensors [222, 223] are relatively simple that the pixel only includes the quench, recharge and readout circuits. Routing to the external counter and TDC modules are required for further TOF or photon counting applications.

More recently, SPAD image sensors have been evolved to include multibit counter/storage [224] and/or high speed RO TDC [212, 225] and/or histogram [226] functionality per pixel/column basis. And custom designed SPAD sensors are developed for specific applications. However, more sophisticated pixels usually reduces the SPAD active area in pixel. In general, for FSI (front side illuminated) SPAD sensor design, a trade-off between photo-sensitivity and pixel functionality is required.

In addition, there are also novel BSI (back side illuminated) 3D- stacked SPAD sensors which have SPAD device on the top layer silicon and pixel circuitry on the bottom layer. 3D-stacking enables a high fill factor (potential 100%) without sacrificing the pixel functionality.

We will focus on the discussion of FSI SPAD sensor due to the limited accessibility of 3D-stacking SPAD sensors.

4.5.2.1 SPCImager

In order to achieve high photo-sensitivity, there are SPAD image sensors employed a minimalistic single-bit pixel. The pixel is implemented either in digital [227] and analogue [61, 228-230] domain. These sensors usually achieve a high fill factor, for example, a 16μm pixel with 61% fill factor in [229]. Due to the limited pixel counting capacity, oversampling is required to reconstruct the image in a different way to conventional sensors.

We have employed a CMOS SPAD image sensor for optical measurements. The Quarter Video Graphics Array (QVGA, 320×240) array image sensor (labelled SPCImager) with 8 μm pixel pitch and 26.8% FF was fabricated in the 130 nm Imaging-CMOS process of ST Microelectronics (Figure 4-16 (a) [61]). By employing analogue counting and binary memory circuit, the in-pixel circuitry reduction enables a small pixel pitch and high fill-factor.

The pixel circuit schematic is shown in Figure 4-16 (b). In analogue photon counting mode, the photon pulses discharge a capacitor which is reset at the initial of a time gate frame. The pixel analogue dynamic range is controlled by the amount of charge for every detected photon. The pixel operation timing diagram is shown in Figure 4-16 (c). The non-uniformity of charge step from one photon to another and from pixel to pixel limits the counter depth and analogue pixel performance.

The image sensor can also be operated as a single-bit dynamic memory with digital readout. Readout noise and quantization noise are negligible. The continuous readout can achieve a frame rate of several kilo-frames per second (kfps). In the binary operation mode, the SPCImager is an example of a fast Quantum Image Sensor. Although QIS pixel state is either 0 (no photon detected) or 1 (at least one photon detected), the sum of these binary values or ‘bit-planes’ in space and/or time provides a spatio-temporally oversampled grayscale image.

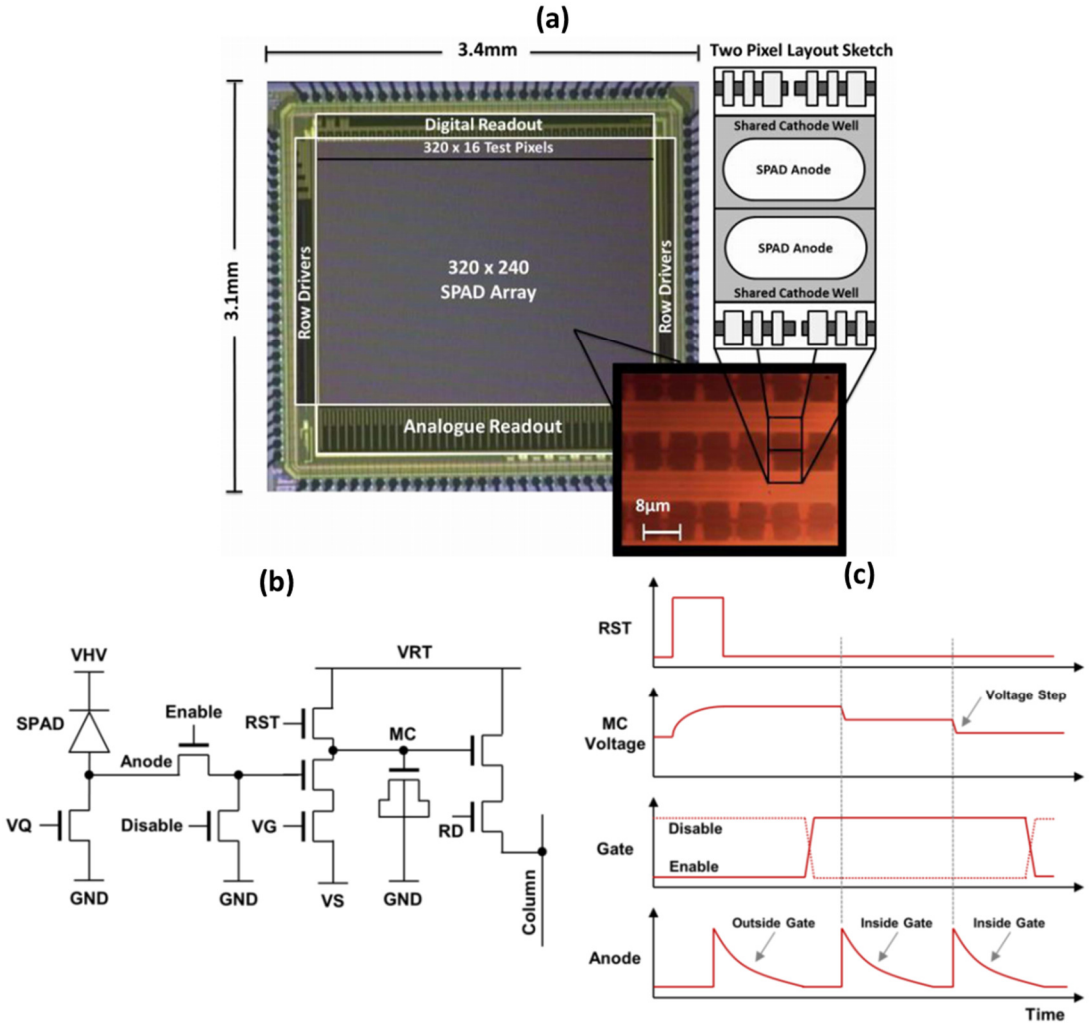


Figure 4-16 (a) Photomicrograph of the SPAD-based QVGA imager, inset: magnification of the pixel array layout with SPAD; (b) Analogue single photon counting pixel schematic diagram; (c) timing diagram [61]

4.5.2.2 Quanta Image Sensor

The tendency of image sensor pixel shrinkage reduces SNR and full well capacity. Fossum et al. have projected the development of CMOS image sensor is towards QIS with sub-electron read noise, sub-micrometre pixel pitch, multi-megapixel resolution and highly oversampled frame rate [231]. The QIS sensor has the advantages of the high SNR and the flexibility of oversampling to expand dynamic range. It is one of the promising options for future image sensor developments.

QIS cameras are different from the standard image sensors which have a linear output proportional to the incident light level. For SPAD QIS cameras, each pixel, also known as jots, has a binary value, where a 0 means no photon detected, and 1 means at least one photon detected. Every binary frame output is, in fact, a "bit-plane" in which displays a scatter of 1's and 0's. Figure 4-17 shows a simulation of photon arrival. With exposure level H = 0.6, the detected number of photons is shown in Figure 4-17

(a), following Poisson distribution. For QIS cameras, the readout is only 1 and 0, the 'bit-plane' with more than one photons are quantised to 1, and the zero-photon bit-plane remains zero.

A bit-plane is limited in terms of image information with 1-bit well capacity. To form an image, one requires to capture a number of bit-planes. These bit-planes can be summed spatially and/or temporally to generate an "image" with the potential for high dynamic range. For the estimation by Fossum in [232], a 10mm 42k × 24k QIS with 1 Giga jots would readout several hundred frames per second. A pixel in the final image can be reconstructed through oversampling of 16 × 16 × 16 jots in a spatio-temporal manner. Moreover, as the summation performed for multiple jots in time and space, the pixel size and frame rate of QIS are programmable unlike conventional imagers.

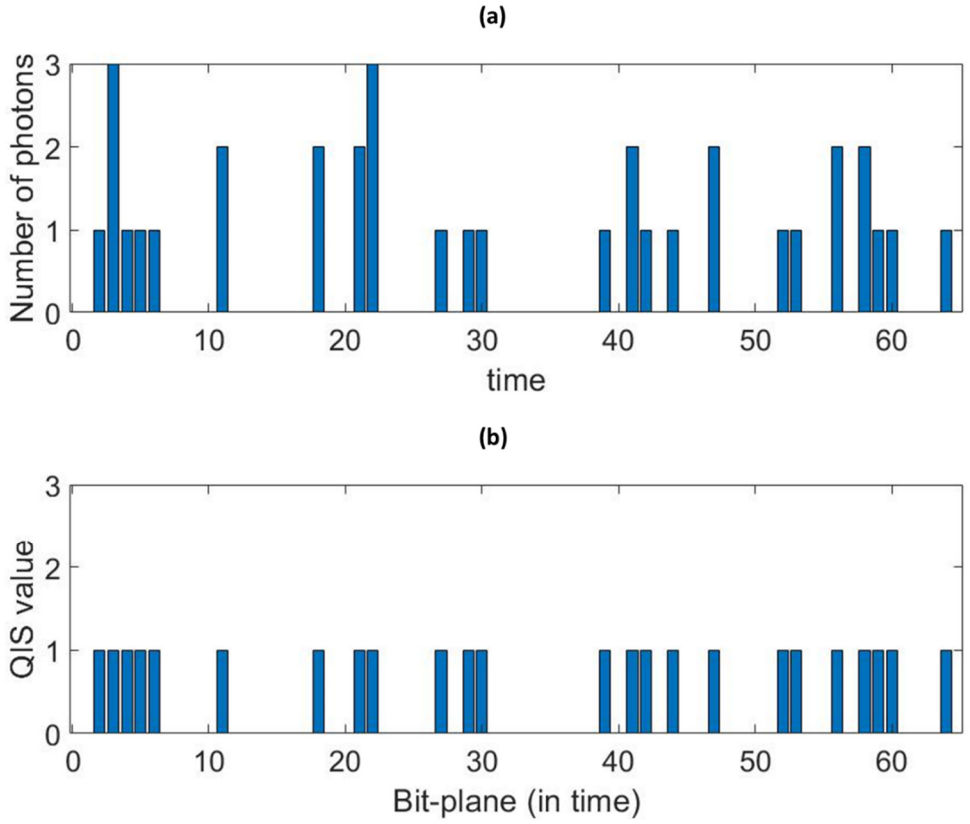


Figure 4-17 (a) Poisson simulation of number of photons arrival with H = 0.6; (b) The simulation value if measured by QIS

- *QIS model*

The incident photons, emitted from the light sources, would arrive stochastically on the QIS sensors following the Poisson process. Analysis of the Poisson arrival statistics is useful to characterise the over different exposure settings and oversampling.

Consider a QIS with quantum efficiency QE, with a photon arrival rate of n, the quanta exposure in a time interval of τ can be described by,

$$H = QE \cdot n \cdot \tau. \quad \textbf{Equation 4-13}$$

It means a number of H photons/photoelectrons arrives at the photodetector on average. In a Poisson process, the probability of photons arriving at each SPAD pixel, i.e. for a time interval of τ, the probability P[k] of k photons arriving is

$$P[k] = \frac{e^{-H}H^k}{k!}. \quad \textbf{Equation 4-14}$$

Therefore, the probability of no photons arriving is

$$P[k = 0] = e^{-H}. \quad \textbf{Equation 4-15}$$

Moreover, the probability of at least one photon being detected is

$$P[k > 1] = 1 - e^{-H}. \quad \textbf{Equation 4-16}$$

Each jot would have two states, and their probabilities can be described by Equation 4-15 for 0's, and Equation 4-16 for 1's. For an oversampling of M jots, the expected number of jots with value 0 is given by,

$$M_0 = M \cdot P[k = 0] = M \cdot e^{-H}. \quad \textbf{Equation 4-17}$$

The expected number of jots with 1's is,

$$M_1 = M \cdot P[k > 1] = M \cdot (1 - e^{-H}). \quad \textbf{Equation 4-18}$$

Therefore, the bit density (average of oversampled bit-planes) can be used to approximate the probability of state 1,

$$D = \frac{M_1}{M} \cong P[k > 1]. \quad \textbf{Equation 4-19}$$

As shown in Figure 4-18, the D – log (H) plot shows an "S-shape" curve which is similar to the D-log response of photographic plate density [233]. For the range of 0≤H≤0.1, the exposure level is low, the bit density approximates the exposure,

$$D \cong H. \qquad \textbf{Equation 4-20}$$

The non-linearity is around 5% when H reaches 0.1. For H = 1, where the linear response saturates, the bit-density D is 63%. Moreover, it is 86% at twice overexposure, and 99.3% at five-time exposure. If the 99% bit-density is considered as the maximum overexposure, the maximum ratio of exposure is 4.6 × H. The exposure can be recovered from the measured bit density through non-linear Equation 4-20.

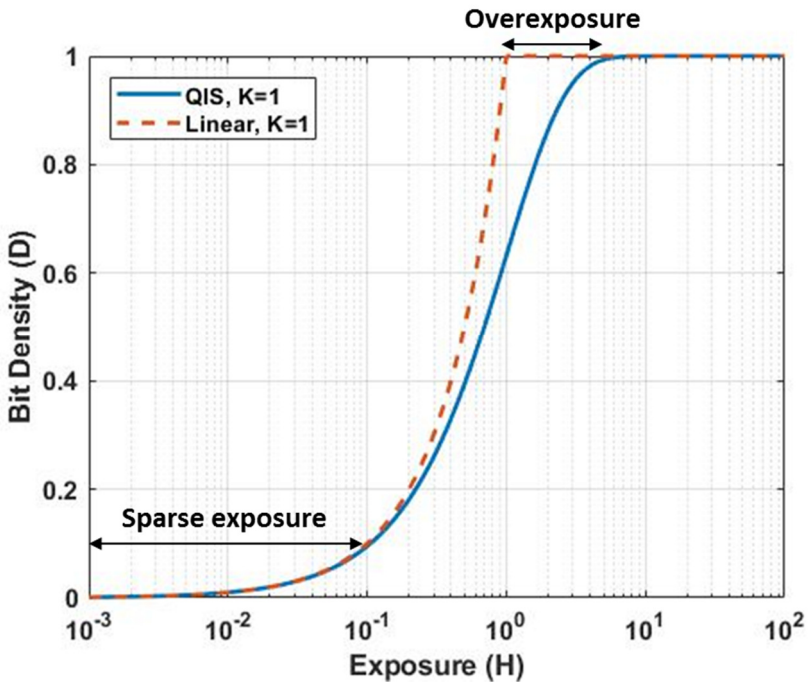


Figure 4-18 D versus log (H) plot of exposure characteristic of QIS (blue line), linear response (red dash)

- **QIS background subtraction**

Unlike common CIS, quantisation noise and readout noise are negligible for SPAD image sensors. However, SPAD cameras suffer from dark noise and thermal induced DCR. Background subtraction can be applied to the recovered exposure level. The measured exposure, including dark count and signal, can be described by,

$$H_{measure} = H_{signal} + H_{dark}. \qquad \textbf{Equation 4-21}$$

where H_{signal} is the signal photon rate, and H_{dark} is the photo induced by dark count. Equation 4-19 can be used to show the measured bit-density,

$$D_{measure} = 1 - \exp(-H_{measure}) = 1 - \exp\left[-\left(H_{signal} + H_{dark}\right)\right], \qquad \textbf{Equation 4-22}$$

$$H_{signal} + H_{dark} = -\ln(1 - D_{measure}),$$

$$H_{signal} = -\ln(1 - D_{measure}) - H_{dark},$$

Another measurement is taken when the incident light source is off,

$$D_{dark} = 1 - \exp(-H_{dark}),$$

$$H_{dark} = -\ln(1 - D_{dark}).$$

Equation 4-23

The exposure signal can be deduced from Equation 4-22 and Equation 4-23,

$$H_{signal} = -\ln(1 - D_{measure}) + \ln(1 - D_{dark}) = \ln\left(\frac{1 - D_{dark}}{1 - D_{measure}}\right).$$ **Equation 4-24**

With time interval τ and quantum efficiency QE, the count rate n can be derived from Equation 4-13,

$$n_{signal} = \frac{1}{\tau \cdot QE} \cdot \ln\left(\frac{1 - D_{dark}}{1 - D_{measure}}\right).$$ **Equation 4-25**

- **QIS signal to noise ratio**

Similar to a conventional image sensor, QIS also suffer from the effect of the photon shot noise. The shot noise is intrinsic to any experiments that follow a Poisson distribution. The variance of the signal is equal to the signal magnitude due to photon shot noise. The variance of the QIS signal, following the binominal distribution is defined by,

$$\sigma_D^2 = M \cdot P[k = 0] \cdot P[k > 0] = M \cdot D \cdot (1 - D) = \frac{M_0 \cdot M_1}{M}.$$ **Equation 4-26**

With Equation 4-15 and Equation 4-16, it can also be described as,

$$\sigma_D^2 = M \cdot e^{-H} \cdot (1 - e^{-H}).$$ **Equation 4-27**

When the signal level is low, D<0.1 (D – log H curve in the linear region), $\sigma_D^2 = M_1$ equivalent to a conventional image sensor. As the exposure level increases, the noise is less than the variance of D. The relative low shot noise is due to the nonlinearity saturation of D. The number of empty jots is small which gives a variance in D.

The SNR of S which is M_1, is defined as,

$$SNR = \sqrt{\frac{M_1}{1 - M_1/M}}. \qquad \textbf{Equation 4-28}$$

The above equation is the SNR of the QIS signal. We can also derive the SNR for exposure,

$$SNR_H = \frac{H}{\sigma_H}. \qquad \textbf{Equation 4-29}$$

Moreover, the exposure noise can be defined as,

$$\begin{aligned} \sigma_H &= \sigma_D \cdot \frac{dH}{dM_1} \\ &= \sigma_D \cdot \frac{1}{M \cdot e^{-H}} \\ &= \sqrt{\frac{1 - e^{-H}}{M \cdot e^{-H}}} \end{aligned} \qquad \textbf{Equation 4-30}$$

The SNR for H is given as,

$$SNR_H = H \cdot \sqrt{\frac{M}{1 - e^{-H}}}. \qquad \textbf{Equation 4-31}$$

Figure 4-19 shows the SNR plot of bit density and exposure. They are close at low exposure (H<0.1) where bit density approximates the exposure. The deviation becomes evident as the exposure increases. With jots filled up quickly reducing the noise, the SNR for bit density 'artificially' increase towards infinite. However, exposure-referred SNR shows a plateau region, then start to reduce as the exposure

starts to be saturated. As bit density headroom limited, a small σ_D would induce a large noise for σ_H. The SNR_H is a more important figure compared to SNR_D for QIS.

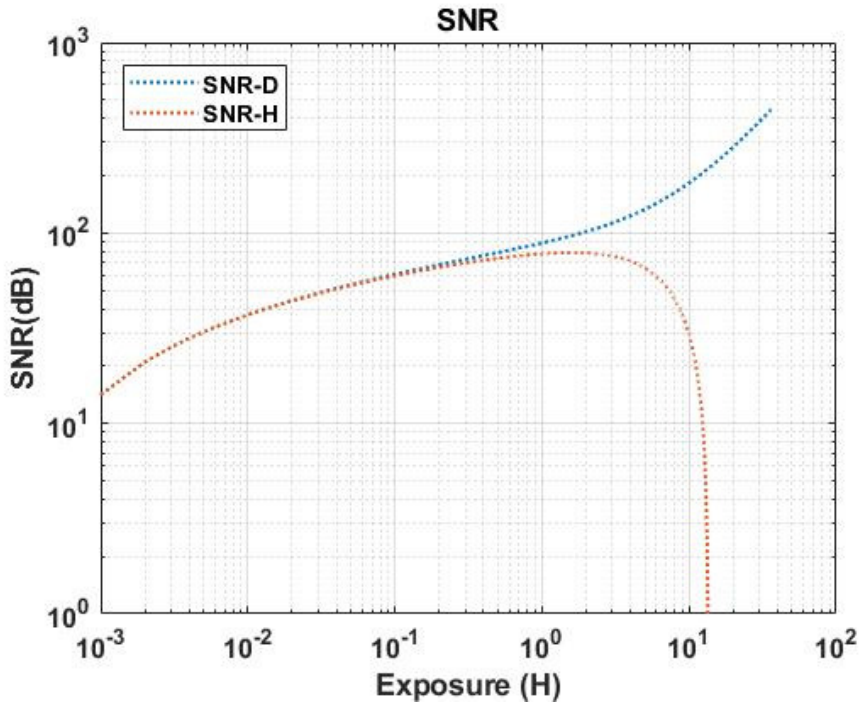


Figure 4-19 Signal to noise ratio for bit-density and derived exposure

- **QIS dynamic range**

The dynamic range can be defined as the ratio between the maximum exposure and the minimum noise-equivalent exposure. The dynamic range is defined as,

$$DR = 20\log\left(\frac{H(max)}{H(noise)}\right) = 20\log\left(\frac{H(max)}{\sqrt{DCR}}\right). \qquad \textbf{Equation 4-32}$$

For SPAD-based QIS, H (max) is interpreted as bit-density reaches 99% of saturation. The value of minimum exposure H (noise) is determined by the DCR level. As the background subtraction is applied, the minimum noise exposure in the dark is the Poissonian noise of DCR which is the square root of DCR.

With a DCR level of ~1,000 cps (median at 60 °C in [205]), an exposure of 100 μs, QE of 10%, H (dark) is 0.00032. Consider H (max) = 4.6, the dynamic range is 20 log (4.6/0.00032) = 83 dB.

To further expend the dynamic range of QIS, one might consider the use of multi-exposure fields with different time intervals. Dutton et al. demonstrate the use of a SPAD QIS with three independent

exposure time and achieve a DR of more than 100 dB with a large high SNR 'plateau' region compared to Figure 4-19 [234].

4.6 Characterisation of OLED microdisplay array using CMOS-SPAD arrays

CMOS SPADs and CMOS SPAD arrays (referred to CMOS SPADs) have addressed a wide range of applications because of the combination of their inherent physical properties – solid state, compact, and robustness along with their impressive performance capabilities – very fast response (dead time in the order of ten nanoseconds [61]), extremely high framerate (up to mega frame per second), single photon sensitivity, and ability to time stamp the instant photon captured. CMOS SPADs have opened the door to dense arrays of SPAD pixels with in-pixel circuitry and on-chip signal processing that can be custom designed and optimised for different applications. The recent applications of CMOS SPADs range from time-of-flight three-dimensional vision [235], and fluorescence lifetime imaging microscopy to imaging of ultrafast physical processes, such as light-in-flight [64].

In this chapter, we discuss and report the use of state-of-the-art CMOS-SPAD arrays for optical characterisation of electronic display pixel arrays. Both a single point sensor (the FlashTDC) and an image sensor (the SPCImager) have been employed for measurement. High dynamic range and very fast transient optical response are observed from the OLED pixel arrays mentioned in Chapter 3. The measurements suggest the advantages of SPAD technology can be used for a broader range of measurements related to displays and other photonic technologies.

4.6.1 Experimental setup

The experimental setup is based on an Olympus BH-2 microscope. The CMOS SPAD sensor (FlashTDC or SPCImager) is mounted through a costumed 3D-printed camera holder. The microscope lamp is used for the SPAD sensor to focus on the array. The setup is shown in Figure 4-20.

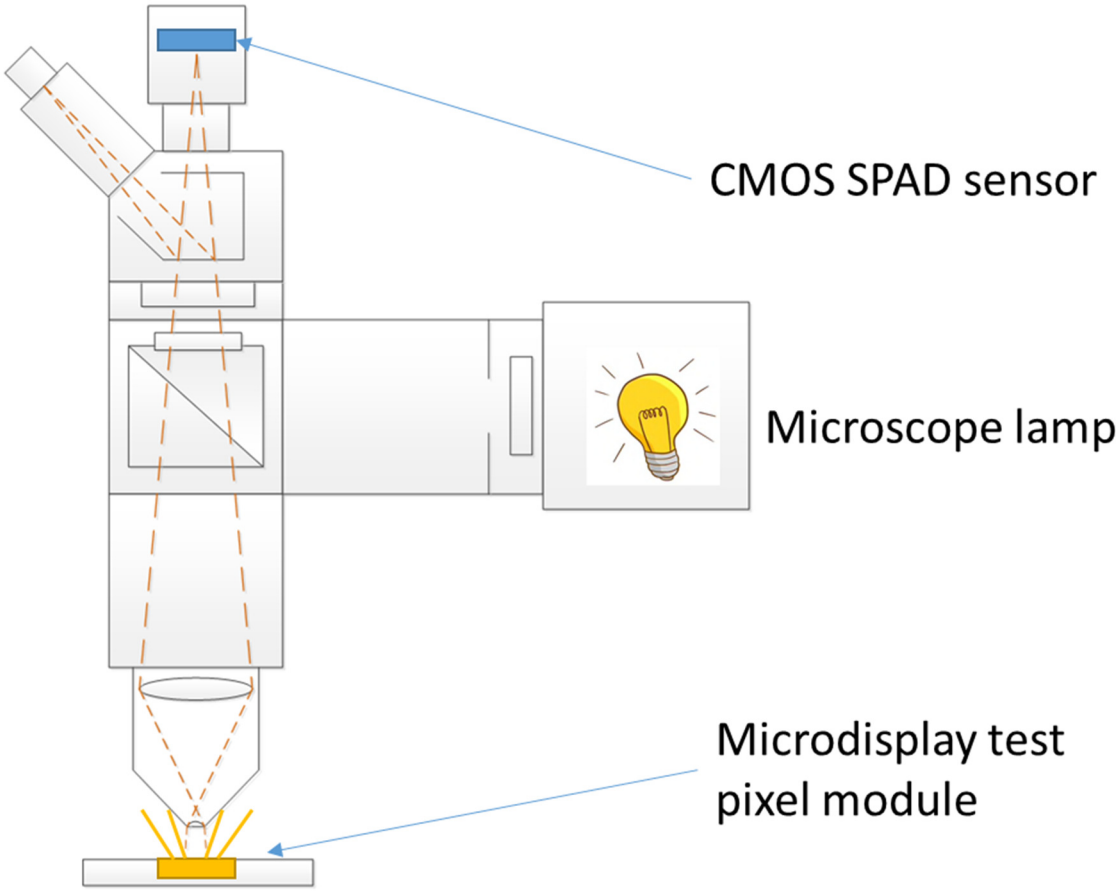


Figure 4-20 Schematic of the measurement setup based on Olympus BH-2 Microscope

4.6.2 Single point sensor measurements

As shown in section 4.5.1, FlashTDC can be used as a single point dSiPM in photon counting mode. The toggle flip-flop XOR tree combination logic allows a photon count rate up to 10 G count per second. Moreover, the minimum signal is the dark noise from the SPADs. As all counts are combined through the XOR tree, dark counts also accumulate during the process. Therefore, we disabled all the high DCR SPADs and only enabled 64 SPADs for measurement. In this case, the dark count is about 1797 cps for each SPAD on average. It is less compared to [205] in the active area is 3.8 times larger. The dynamic range of FlashTDC can be up to 135 dB.

The first measurement is performed for the convention two-T source follower pixel. The pixel operation and electrical measurement are discussed in Chapter 3. The pixel schematic is shown in Figure 4-21.

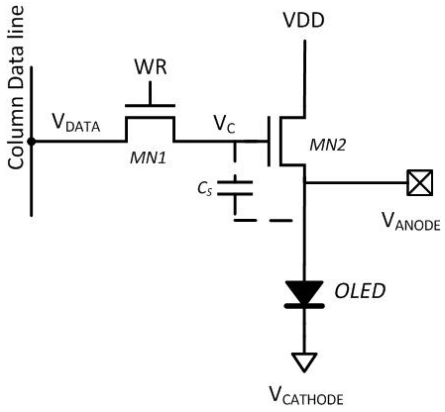


Figure 4-21 two-T source follower pixel schematic

One of the interesting behaviours for this pixel is the leakage induce flicker of sample-and-hold storage point V_C. As we discussed in section 3.5.1.2, the leakage can be lessened by increasing the OFF voltage of V_{DATA}. It can be measured via electrical measuring the OLED Anode voltage. However, the electrical measurements do suffer from the extra parasitic capacitance of the wires and the analogue IO pad, as shown in Figure 3-36. The best way is through optical measurements which measures the luminance level directly from the pixel.

Figure 4-22 shows the optically measured photon count rate from the FlashTDC with the 2T SF pixel configured at 25 Hz. The first frame V_{DATA} is 4V, and V_{DATA} is 0V in the next frame to reset the pixel to the initial state. Background subtraction is also performed removed the dark count level. In order to reduce the photon shot noise, each measurement is taken for 6.5 seconds. Therefore, each cycle of the results in Figure 4-22 is oversampled 40 times. The SNR of oversampled photon counting signal becomes,

$$SNR = \frac{N \cdot S}{\sigma(N \cdot S)} = \frac{N \cdot S}{\sqrt{N \cdot S}} = \sqrt{N \cdot S}. \qquad \textbf{Equation 4-33}$$

where N is the number of times oversampling. The SNR becomes $\sqrt{N}$ times larger than the original SNR.

As shown in Figure 4-22, the flicker leakage reduces to around 11% (after the SF pixel settled from charge injection of switch opened), as V_{DATA} (OFF) increases to 100mV. A reversed biased of 90mV would give leakage of 27% over a 40ms period.

Figure 4-23 shows the leakage measurement compared simulation result from Figure 3-18. The optical flicker is calculated by the photon count difference between 1ms (avoid charge injection effect) and the 10ms (the measurement time of the simulation). Measurement and simulations are close at high V_{DATA} (OFF) where the leakage level is small. The difference at high leakage level is likely caused by the nonlinearity between the OLED anode current (electrical) and luminance level (optical).

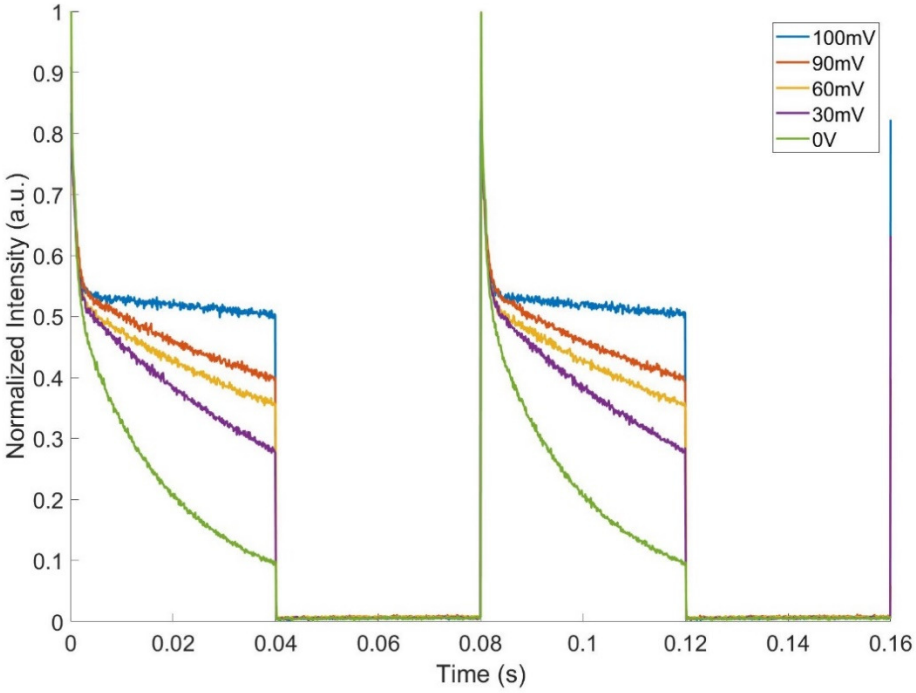


Figure 4-22 Leakage induced optical flicker of 2T SF pixel measured by the FlashTDC, with V_{DATA} (OFF) = 100, 90, 60 and 0 mV.

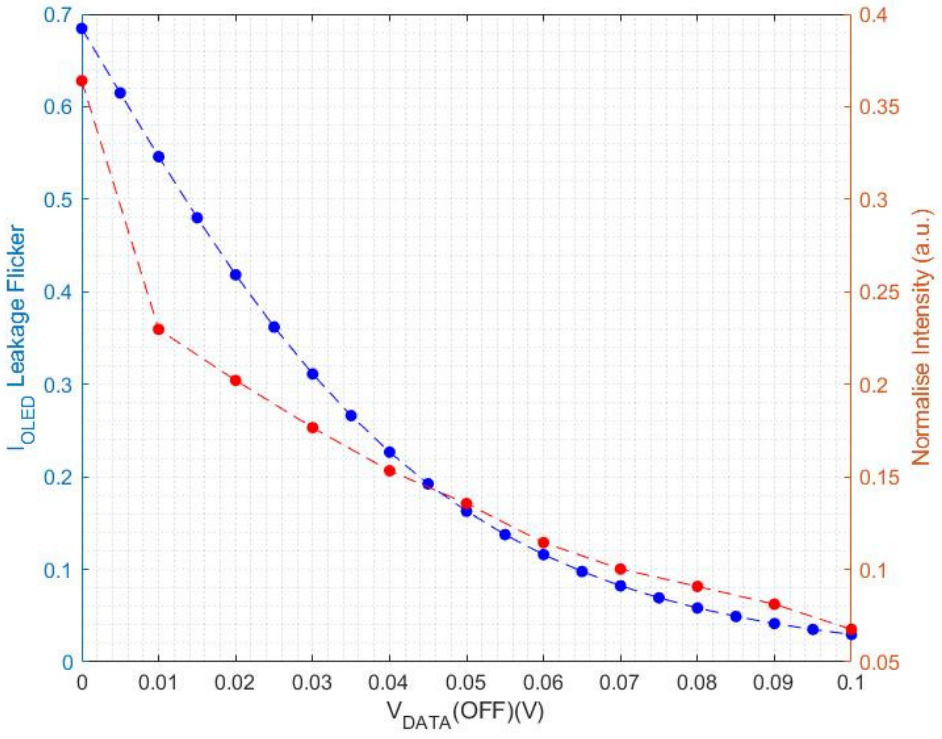


Figure 4-23 Leakage induced optical flicker (at 10ms) of 2T SF switch pixel with regular switch optical measurement (red) vs simulation current (blue).

The need to reverse bias V_{DATA} to reduce leakage would limit the dynamic range of SF pixel. Thus, the annular transistor switch is introduced in section 3.5.1.3. The circular shape transistor removes any edges and reduces the leakage. It has been demonstrated in the electrical measurement Figure 3-37. However, the electrical measurement suffers from parasitics. A direct comparison through optical measurement between the standard transistor and the annular transistor as a switch is provided in Figure 4-23. The leakage of the annular switch with 0V is about 16% which is less than the leakage of regular switch with 90mV reverse bias.

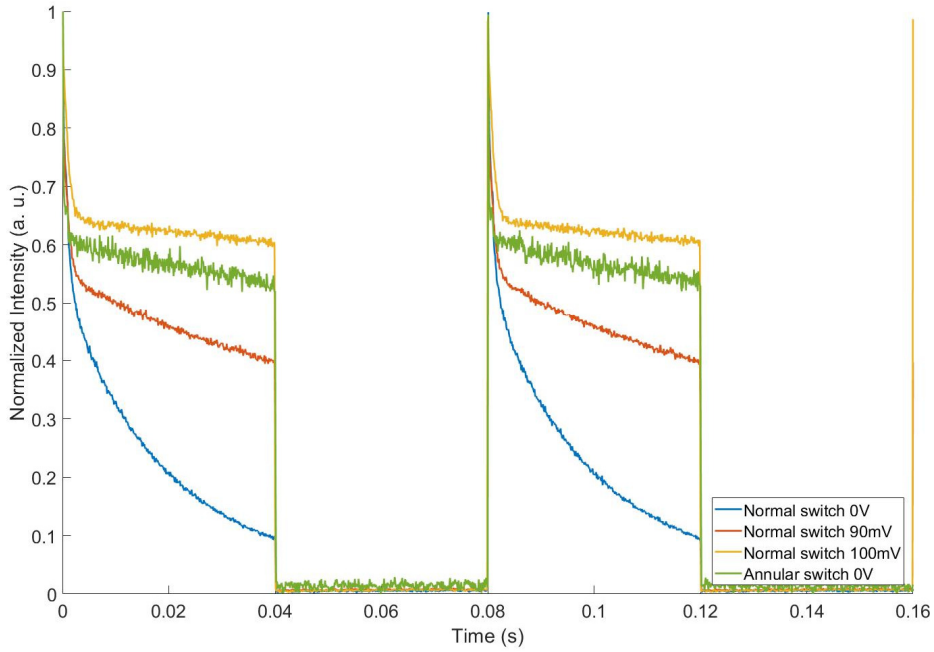


Figure 4-24 Leakage induced flicker comparison between regular switch transistor switch with V_{DATA} (OFF) = 100, 90, 60 and 0 mV, and annular shaper switch with 0 V V_{DATA} (OFF)

Measurements are also performed for different reverse bias voltages of the annular switch SF pixel, as shown in Figure 4-25. However, the leakage level does not have a significant variation. It suggests the leakage mechanism of the annular pixel can be different from a standard transistor. As the discussion shown in section 3.5.1.2, the leakage of a standard transistor induced by the subthreshold current between drain and source terminal is sensitive to the gate-source voltage. If the subthreshold current is not the dominant mechanism, the leakage flicker will not make much difference. In this case, the leakage through the bulk could be the main contributor to the leakage for the annular transistor. It is not affected by increasing V_{DATA} (OFF) to bias a negative V_{GS}. Detail analysis of the leakage of the annular transistor would require TCAD software (e.g. Synopsys) to provide extra information of the device operation.

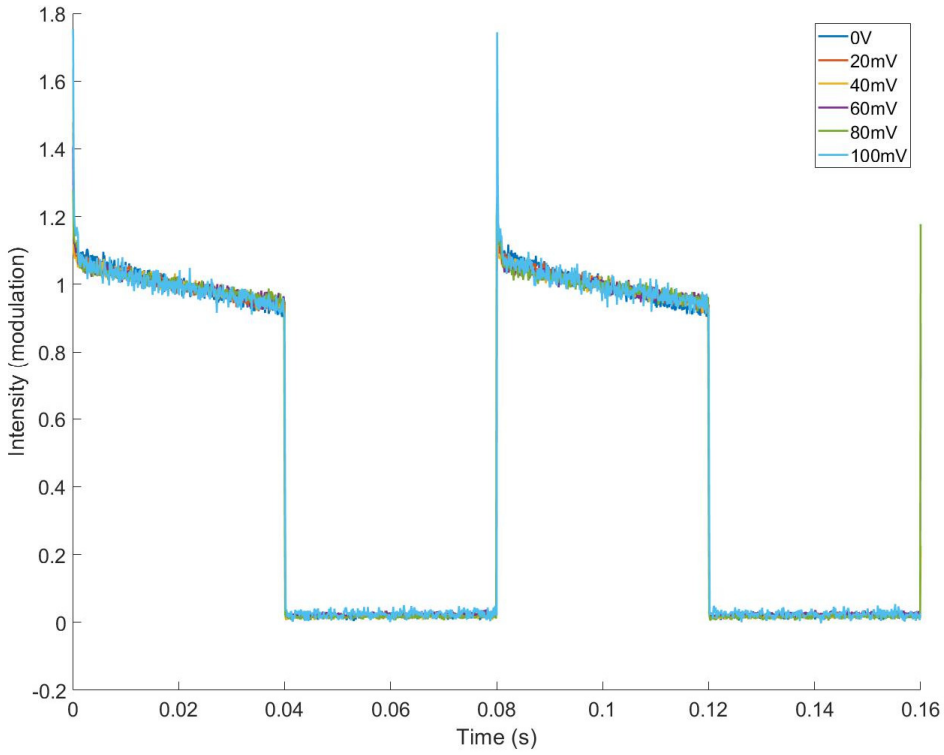


Figure 4-25 2T Source follower pixel with annular transistor switch with a reversed bias of 0, 20, 40, 60, 80 and 100mV.

The FlashTDC measurement suggests it is promising to use SPAD-based dSiPM with high bandwidth (count rate) and fast frame rate. However, due to the inherent dark count, the sensor dynamic range degrades with an increasing number of SPADs. Thus, only 64 SPADs are included in the measurements. The reduced number of SPADs has a limited active area. Besides, the magnification of the microscope setup is constraint, which the microscope field of view is much larger than the SPAD sensor active area. The OLED pixel arrays are also with a small pixel pitch. It is non-trivial to achieve a well focus within the field of view of the SPAD sensor. Figure 4-26 shows the variation of photon counts of three tests with the same setup, but performed in different occasions.

This is also a common issue for other single point sensor measurement setups. It is usually resolved by a more complex optical setup or measurement for large panel display which the field of view is much less than the region of interest.

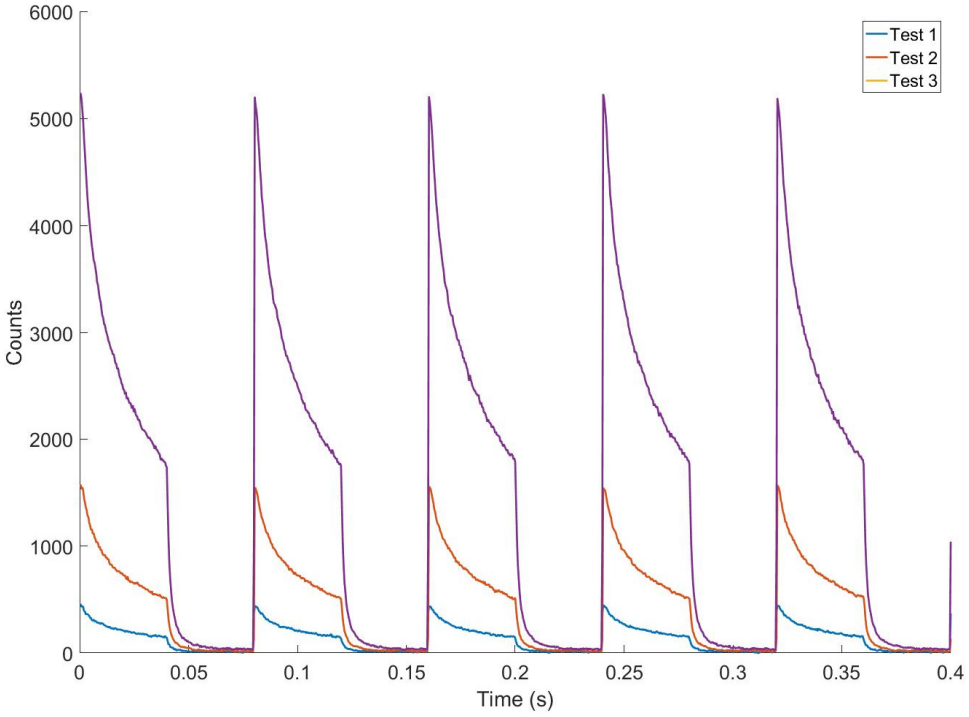


Figure 4-26 Measurements with the same configuration but with different focus

4.6.3 SPAD Imager Measurements

For measurements that required 2D information, such as non-uniformity, crosstalk, the image sensor is preferred to single point sensor. Conventional image sensors (e.g. CCD or CMOS) usually have limited performance, in terms of frame rate, dynamic range and SNR. A binary SPAD camera could be a preferable sensor for this application. There is a negligible level of readout noise associated with digital SPAD QIS. Although, there is only one bit information available each pixel, it can still achieve a high dynamic and high SNR through bit-plane oversampling as we shown in section 4.5.2.2. On the other hand, the logarithmic compressed measurement data is only 1 bit per pixel. The amount of measurement data each frame is cut down. The binary SPAD camera captures a frame at a higher rate compared to conventional CCD and CMOS imagers. SPCImager allows a frame rate of more than 10k fps (binary). The binary frames can be post-processed through oversampling and the frame rate can be adapted accordingly. Besides, the frame rate can be further increased by selecting a region of interest (ROI) to minimise the data transmission. Options of both rolling and global shutter modes are available. Global exposure mode is used in most measurements to synchronise the exposures.

Figure 4-27 demonstrates a raw bit-plane image of the OLED pixel array showing a letter ‘E’. The bit-plane has some jots reporting at least one photon with logic ‘1’ and no photon with logic ‘0’. Figure 4-28 shows six temporally oversampled QIS images. The number of oversampling bit-planes increases in quadruple, whereas the equivalent exposure time is also quadruple for the images. The signal level of each pixel is extracted with background subtraction through Equation 4-24. The frame rate is, therefore, quartered as the number of images required to output an image.

Hot pixels (also known as high DCR pixels), which have more than 5,000 counts per second at the background frames, are removed. The median value of the peripheral pixels is interpolated to the hot pixel to create an image.

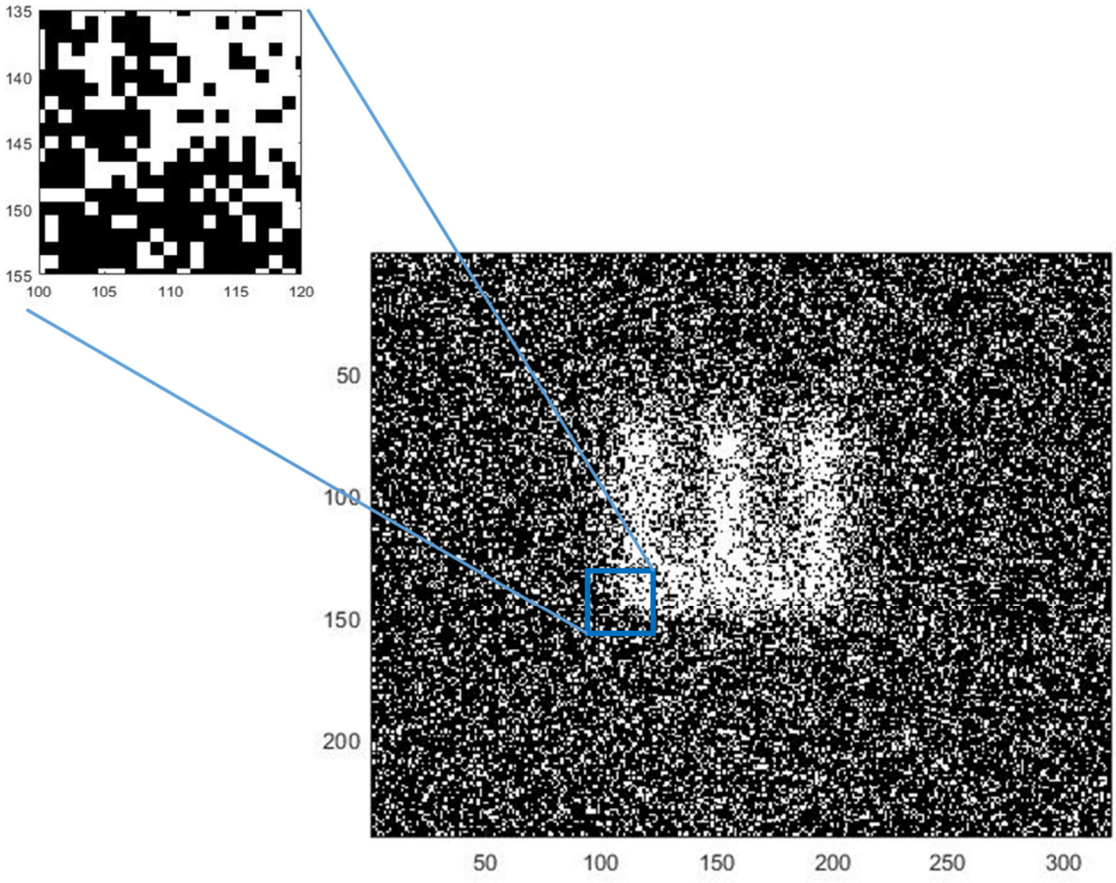


Figure 4-27 One raw frame from SPCImager, '1' means at least one photon arrival, '0' means no photon arrival, captured at 100 μs exposure, 3410 fps; inset: zoom in of the QIS bit-plane.

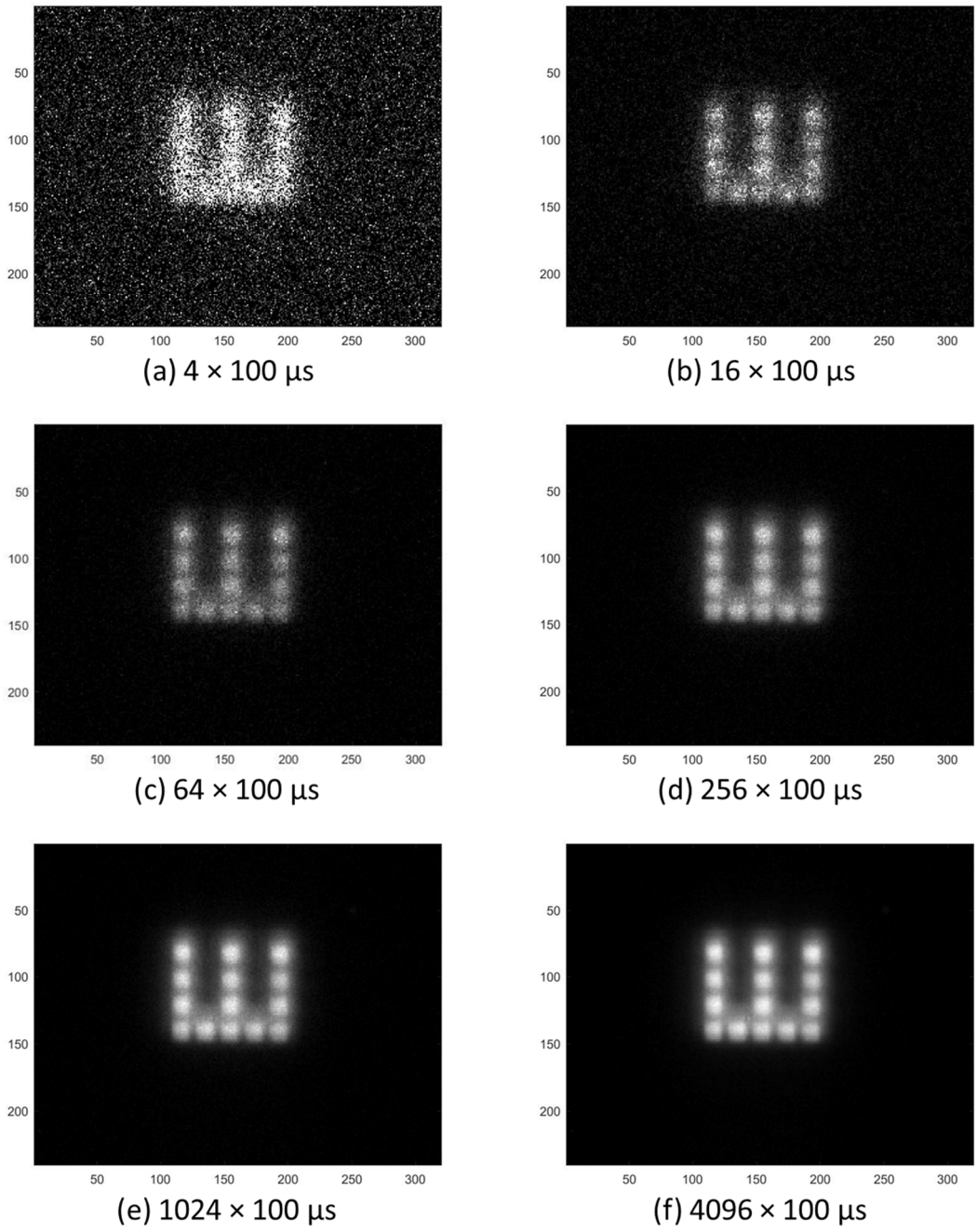
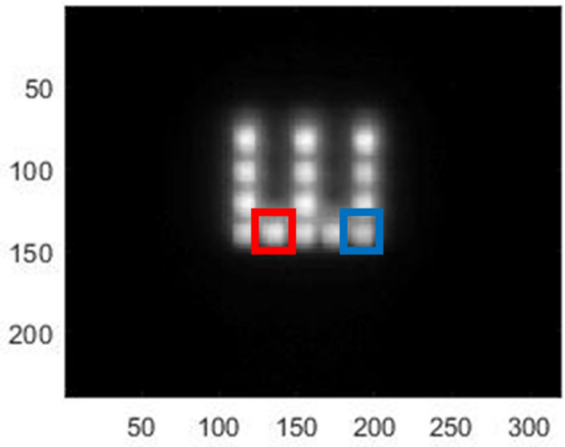


Figure 4-28 Digital oversampling in the time domain, accumulating successive bit-planes to create an oversampled image, six images are shown with the respective exposure time.

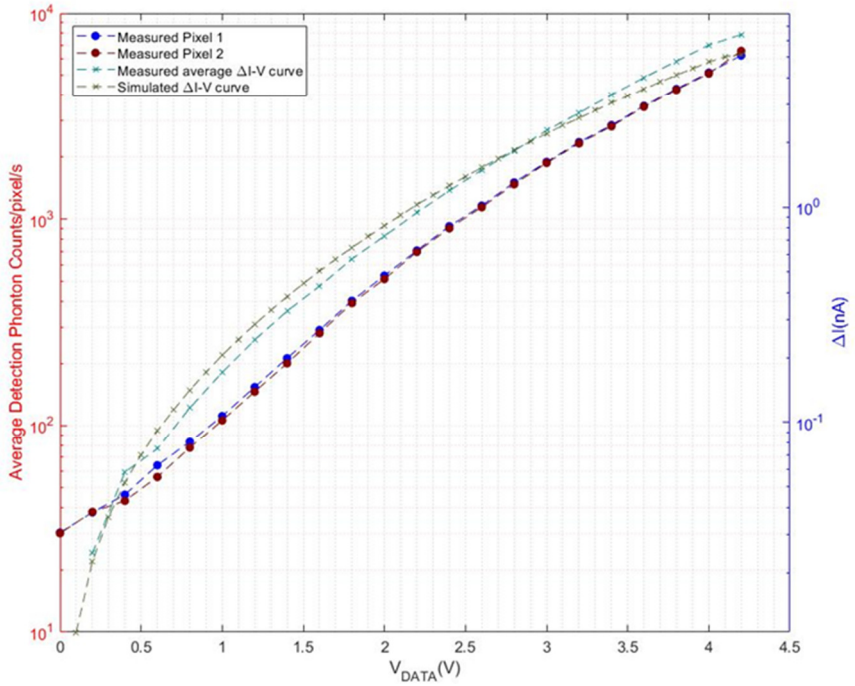
4.6.3.1 High Dynamic Range Steady State Measurement

A demonstration of DC steady-state non-uniformity measurement is performed. The source follower OLED pixel array (section 3.6.1) is employed. In the capturing image shown in Figure 4-29 (a), an OLED SF pixel with 4.7 μm pixel pitch is optically mapped onto approximately 324 (18 × 18) SPAD pixel (8 μm pixel pitch). The comparison of measured photon rate of two SF pixels (Pixel 1 located in the blue box, and Pixel 2 located in the red box in Figure 4-29 (b)) versus the sweep of V_{DATA} is shown in Figure 4-29 (a). The incident photon rate level is derived through Equation 4-24 with 1000 × temporal oversampling and 400 spatial binning (averaging). Since the white OLED has a broad spectrum and there is no emission band-pass filter applied, the quantum efficiency and pixel fill factor of the SPAD pixel is not considered.

The OLED current is measured from the cathode current of the pixel array divide by the number of the illuminated pixels (same as Figure 3-35). As it is discussed in section 3.6.1, the measured pixel current suffers from a static leakage (pixel current is not 0A at 0V). The difference of pixel current and 0V current ($\Delta I = I - I_{0V}$) are plot instead. It can be found that similar luminance with small mismatch across the different V_{DATA} voltage between the two pixels. The curves of the measured photon counts and pixel current (both measured and simulated) are closed. The difference can be attributed to the nonlinearity of the pixel current and the OLED luminance which is not included in the OLED model yet.



(a)



(b)

Figure 4-29 (a) SPAD image of OLED pixel array (1000 oversampled field with 100 µs exposure); (b) Sweep of DATA voltage (x-axis) versus derived incident photon rate of pixel 1 (blue circle marker) and Pixel 2 (red circle marker) (left y-axis), measured average OLED pixel current and simulated pixel current (right y-axis). Pixel 1 locates in the blue square, and Pixel 2 locates in the red square in (a)

4.6.3.2 Fast Transient Measurement

Another measurement is for the analogue PWM pixel aiming at capturing fast transient behaviour of the OLED pixel. The PWM pixel, as we have shown in section 3.5.2, is configured to work in Pulse-Coded Modulation (PCM) mode. The multi-bit storage capacitor in Figure 3-21 is employed as a single-bit dynamic memory. The OLED pixel is switching between ON and OFF each frame (Row Write). The imperceptibly-fast binary switching of the OLED produces the visual impression of a grey scale at each pixel. In theory, the perceived grey scale is proportional to the on/off time ratio of each frame. Moreover, the luminance level is consistent (uniform) during each pulse, and from pulse to pulse.

The OLED pixel array is driven at a frequency of 1 kHz, with one frame OFF and the next frame ON, 50% duty ratio. The SPAD array measures in global shutter mode, with a frame rate of 10 kfps. During each 100 μs frame, there are 65 μs for exposure and 35 μs for transmission and pixel reset. In order to achieve a high frame rate, the SPCImager is capturing with a reduced resolution of 80×320, and the ROI is only the area that has the active OLED pixels. The SPCImager captures around 20 frames for each display frame of the OLED pixel array.

Figure 4-30 shows four captured raw bit-planes. As it is displayed, the ON/OFF of each row of pixels is inserted in a column-by-column manner. The letter ‘E’ is updated column by column with one frame ON and one frame OFF. As the update rate is high, it should be perceived as half luminance for the whole frame by the observer in most cases. A graph of the total photon count is shown at the bottom of each frame, plotting the luminance level versus time.

Similar to Figure 4-27, the raw bit-plane shows a noisy image with only 1-bit information. The dynamic range and SNR are very limited without any oversampling. However, it samples at the highest frame rate, reflecting a real-time transient behaviour of the OLED pixel array.

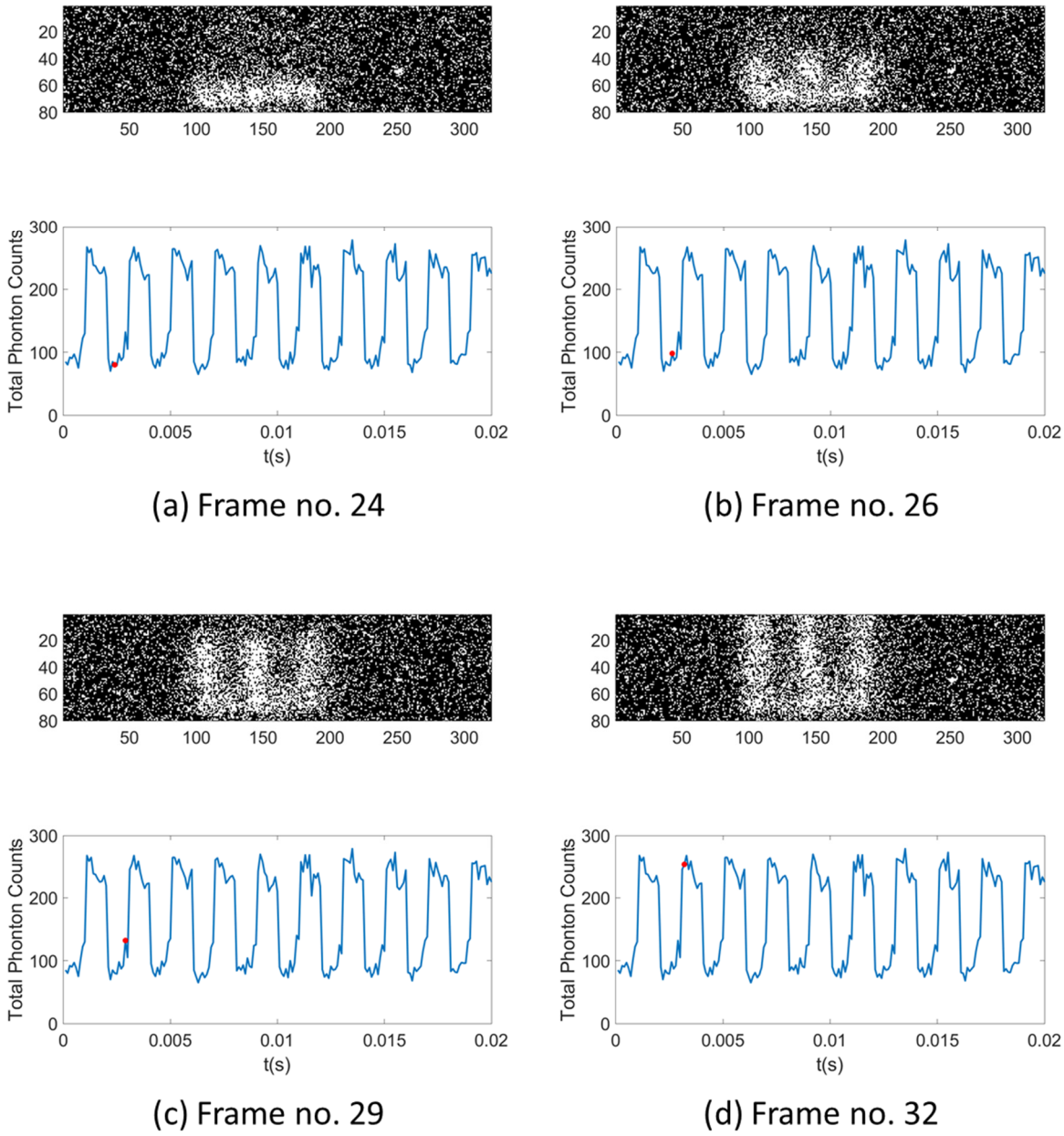
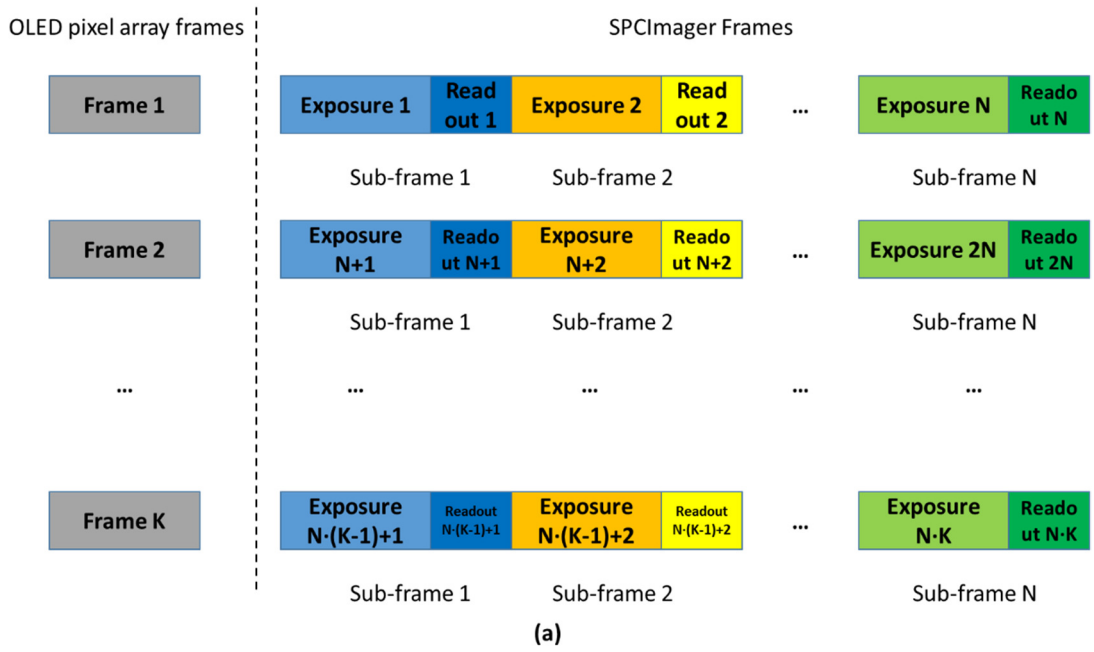


Figure 4-30 Example of four raw bit-planes captured by SPAC imager at a frame rate of 10 kfps, 65 µs exposure; the detected total photon count is plotted against time at the bottom of each frame, the red circle indicates the photon count of the current frame.

Capturing a single bit-plane only provides limited information for the transient response. The signal is degraded due to the photon shot noise and the dark counts. Hence, we introduce a technique of oversampling a periodic signal.

As shown in Figure 4-31 (a), if the SPCImager (or other QIS camera) is sampling at a frequency of N (N is an integer) times of the display frame rate. The SPCImager captures N frames for each display

period. Assuming the same content is repeated for K display frames, the bit-planes that captured at the same display frame can be treated as sub-frames. The sub-frames that located at the same "time" position over a display frame should be exposed to the same luminance. Therefore, the same sub-frames can be oversampled. For capturing of N×K, the bit-planes can be oversampled by maximal K display frames. Figure 4-31 (b) shows the photon count plot that can be split by display frame and each sub-frame can be oversampled individually.



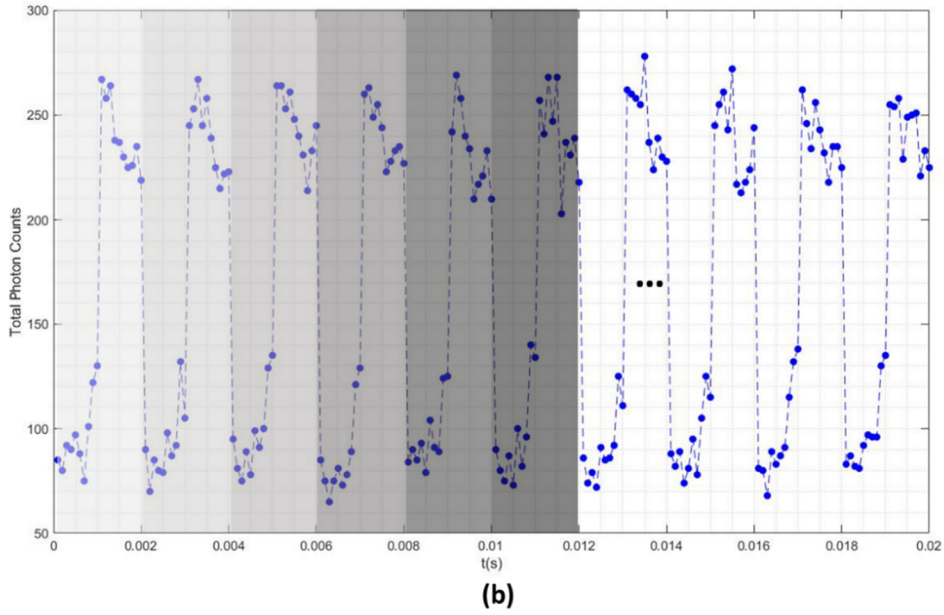


Figure 4-31 (a) Timing diagram of capturing N*K image frames at K display frames; N sub-frames are captured within each display frame; (b) splitting and oversampling the bit-planes in time accordingly

By employing the method mentioned above, Figure 4-32 shows the result after 500× temporal oversampling. The detected photon number can be derived from the QIS model Equation 4-24. From the photon count plot, small overshoot behaviour can be observed – whenever a row of pixels are turned on, the photon counts overshoot to a higher level and settles at a lower level at the next frame. However, due to the frame rate limitation, each measurement point is sampling at 10 kHz, the overshoot behaviour is averaged. Higher frequency measurements are required to assess the overshoot level and its influence on the overall pulse.

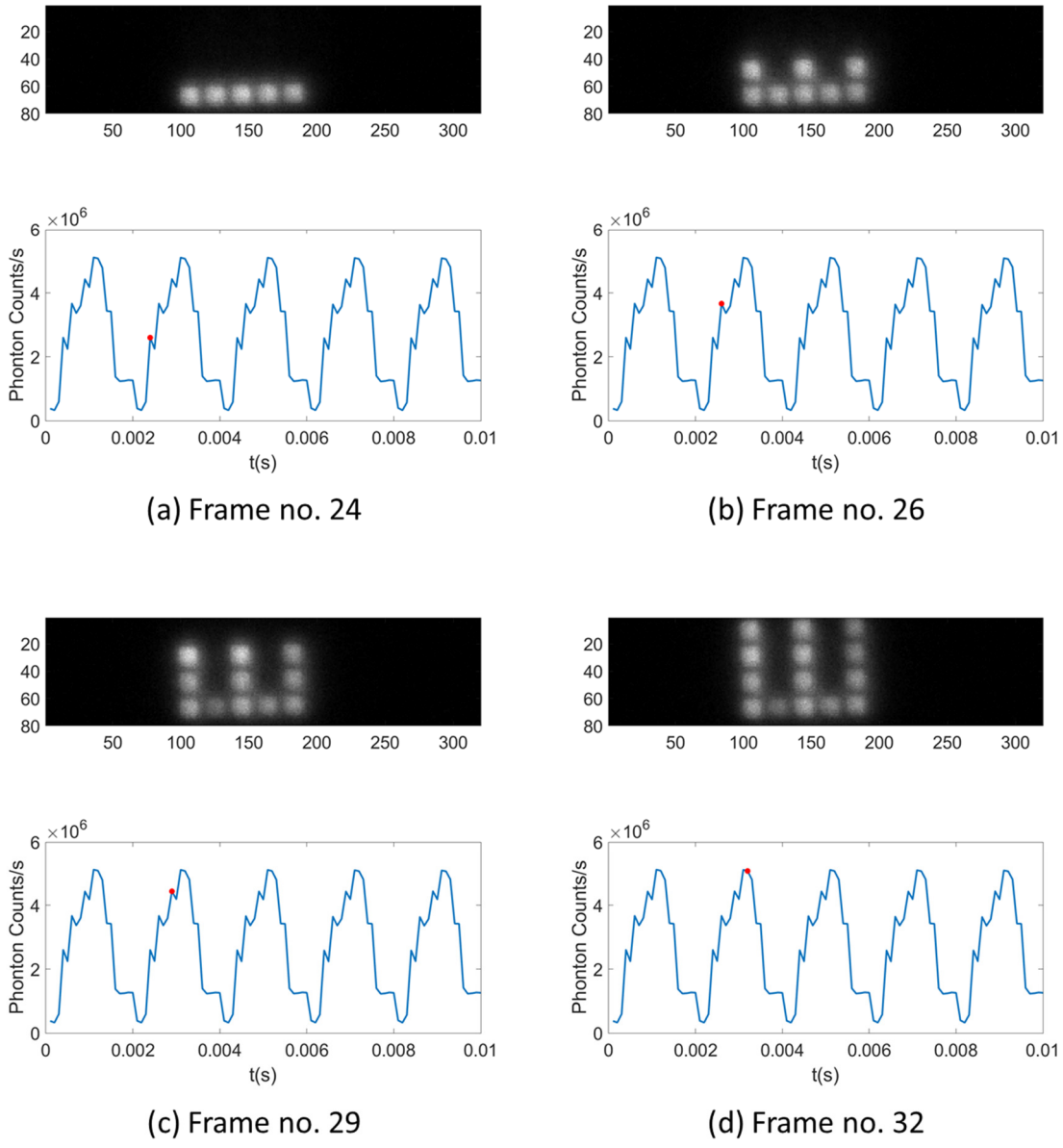


Figure 4-32 Four images at the same sub-frame location as Figure 4-30 post-process through 500× oversampling, total capturing time 5 second, exposure 3.25 second. The photon count plot below each figure is the total photon count derived from QIS model

In order to achieve a higher frequency frame rate, the ROI is sacrificed to only one row of OLED pixels, equivalent to around 20 lines of the SPCImager pixels. The frame period is 20 µs, 10 µs for exposure and 10 µs for readout and reset. The OLED pixel is programmed by an 8-bit, 100 Hz PCM scheme. 500 sub-frames are captured for each OLED pixel display frame. The SPCImager captures 90,000 frames for 1 second. The bit-planes are oversampled by 100 times. Figure 4-33 shows two example frames from the measurement results. The frame of the overshoot point is shown in Figure 4-33 (a). The frame of a settled luminance is shown in Figure 4-33 (b). The top image shows the original linear image and the image shown in the middle column has been applied with Gamma correction ('sRGB').

It is evident that the OLED pixel luminance is not constant during each coded pulse. Overshoot and decay behaviour is shown when the pixel is switched ON from OFF. There are several factors that could contribute to the turn-on overshoot in OLEDs, for example, transient charge imbalance [236, 237], recombination of pre-trapped charges [238], and singlet–triplet quenching [239]. The turn-on overshoot usually happens in the scale of microseconds, then settles to the constant level. It is likely to go undetected by measurement systems with measurement time slower than one millisecond.

It can be seen that the photon counts of the overshoot frame are more than twice of the settled frame. For this reason, the settled frame at the linear scale is unnaturally dim, whereas the Gamma corrected images are optimised.

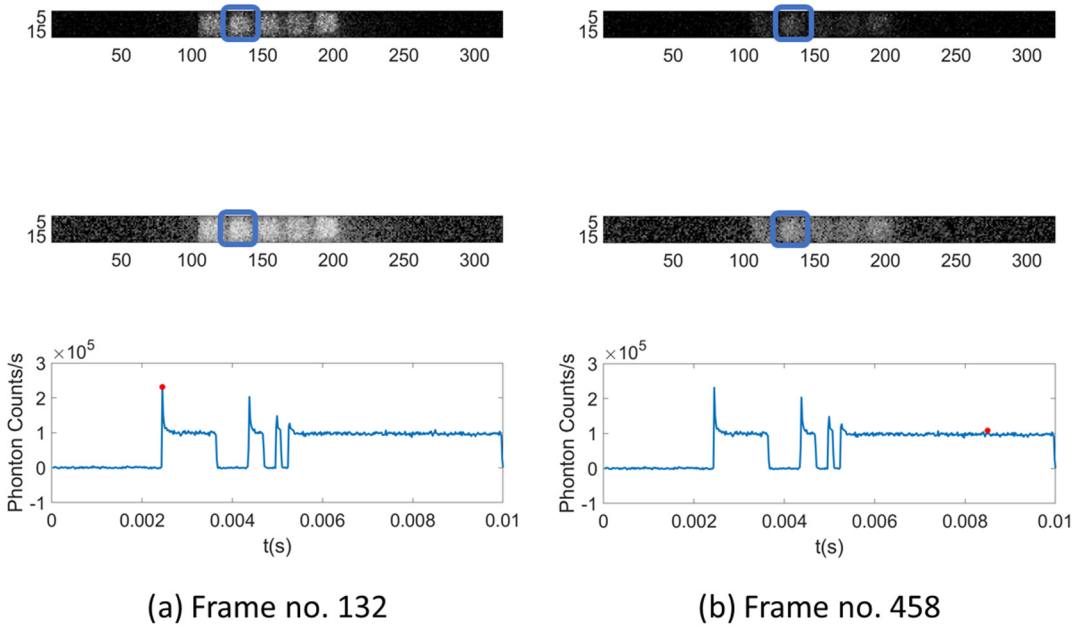


Figure 4-33 Measurement of PCM OLED pixels with 20 µs frame time (10 µs exposure, 10 µs readout and reset), (a) frame no. 132 and (b) frame no. 456 in time; 100× temporal oversampling has been applied; the top image is in linear scale, and middle image is with sRGB Gamma correction, the bottom graph is the derived photon count level of the OLED pixel located in the blue square.

In order to study the relation between the overshoot behaviour and OLED pulse width, two PCM scheme – 8b'10101010 and 8b'01010101 are applied to generate different pulse width. The transient photon counts measurement of the two pixels in the same locations as Figure 4-29 (a) are presented in Figure 4-34 (a) and (b). The number of photon counts/pixel/s is reconstructed through oversampling 100× temporal oversampling. The two pixels are with similar transient response, small discrepancies are found at the turn-on overshoot level.

To quantify the amount of overshoot, we take the integration photons of each pulse ($H_{overshoot}$) and divide it with the photon number of the pixel that is set ON over a full frame (H_{ON}). In this case, the OLED pixel drives a constant ON voltage. It does not show any turn-on overshoot behaviour. In Figure 4-34 (c), the ratio of overshoot to signal is plotted versus different pulse widths with 8ms, 6ms, 2.5ms OFF time of pixel 1 and 2.5ms OFF time of pixel 2. There are two conclusions that can be drawn from the measurement. The first is the shorter is the pulse, the more is the luminance deviation. Longer pulse is less susceptible to the overshoot effect. The second is the magnitude of the overshoot is relating to the OFF time before it is switched ON. The longer the OFF time, the greater is the luminance overshoot. While the transient responses of pixel 1 and pixel 2 with the same OFF time are similar, any small variation in the overshoot level would cause considerable luminance mismatch at short pulse width.

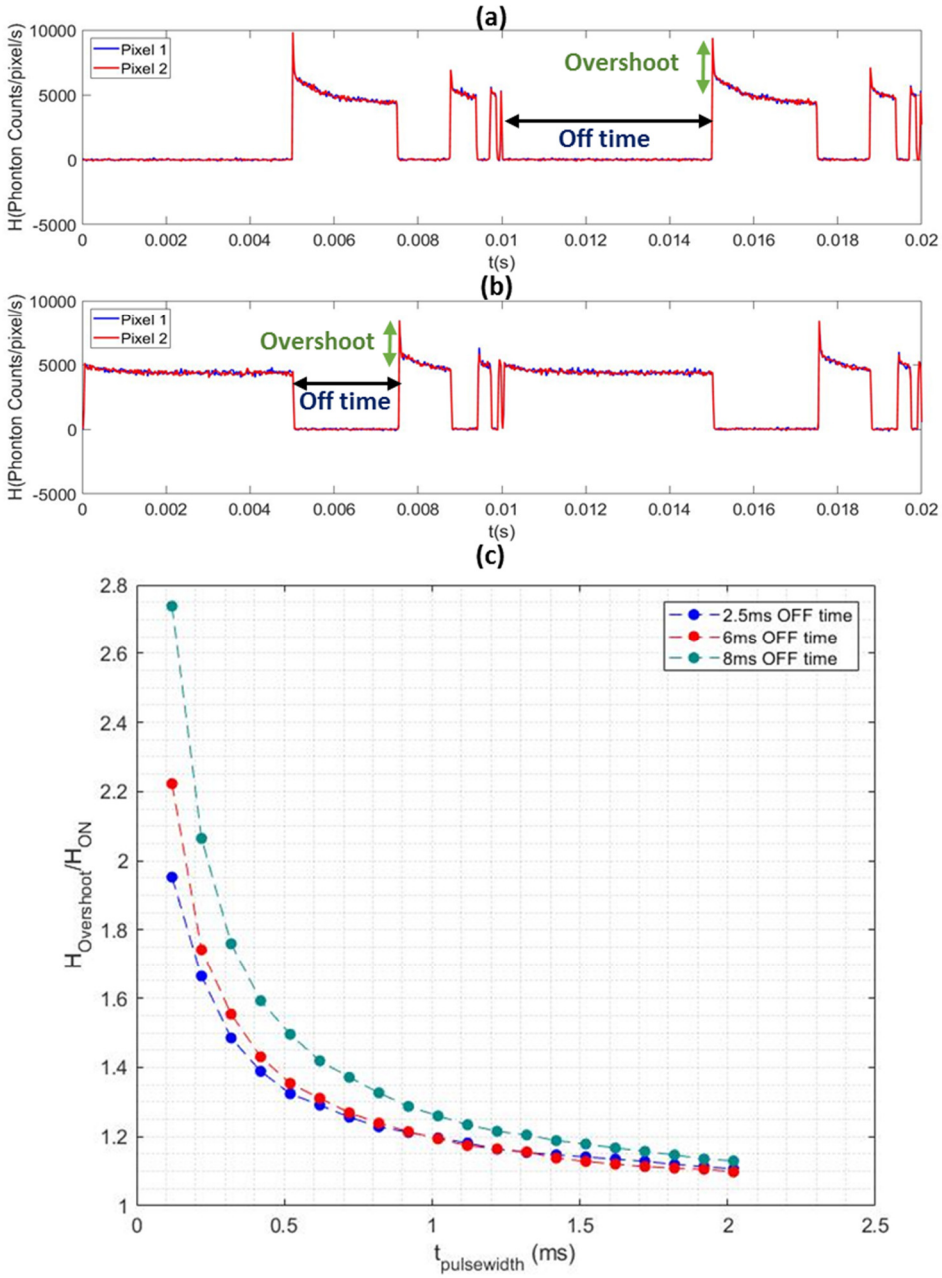


Figure 4-34 PCM pixel transient measurement of 100 oversampled field (a) encode 8'b10101010 and (b) encode 8' b01010101 of pixel 1 (blue), pixel 2 (red). (c) The ratio of overshoot (the photon count magnitude of maximum overshoot point to the magnitude settled emission) versus pulse width with OFF time of 8ms (green circle), 6ms (red circle) and 2.5ms (blue circle).

4.7 Summary and Conclusion

Optical experiments that employ SPAD sensors to characterize OLED pixels arrays that designed in Chapter 3 have been presented. Two CMOS SPAD sensor devices are applied – the FlashTDC configured in photon counting mode as a single point sensor and the SPCImager configured as a QIS imager. Both sensors are developed for the purposes of TOF and/or FLIM research. However, the theoretical model and the experiments show that the SPAD sensors can match or even exceed the performance of conventional luminance sensors.

The Flash TDC sensor has been applied for the OLED pixel flicker measurements. Without any electrical interference, the measured optical flicker is close to the simulated and measured OLED pixel current response. Table 4-1 lists FlashTDC comparing with a commercial PMT-base measurement sensor GLRT[38] and a spectro-radiometer published by NPL. GLRT biases the PMT in analogue mode and employs a fast ADC (500 kHz) to convert the analogue output to 16-bit digital output. However, analogue readout of the PMT suffers from the offset, ripple noise and ADC quantisation error. On the other hand, readout noise and quantisation noise is negligible for digital SPAD sensors. For comparison with PMT in photon counting mode, thanks to the toggle flip-flop with XOR tree structure, a higher dynamic range is achieved by FlahsTDC. Also, cooling can be introduced to reduce the dark count level approximates PMT. Besides, the microscope – based measurement system can be improved for focusing the field of view of the FlashTDC sensor and OLED pixel array.

[38] Gray Level Response Time Measurement Kit, Westar Display Technologies, Inc

Table 4-1 Single point sensor specification comparison between PMT and FlashTDC

Measurement system	**GLRT [240] (Hamamatsu H10722-110)**	**NPL PMT Spectro-radiometer [182]**	**FlashTDC (this work)**
Sensor technology	PMT	PMT	SPAD dSiPM
Sampling rate	500 kHz	n/a	188 kHz (Minimum 5.3µs readout)
Dynamic range	n/a	10 – 10^7 photon counts/s (Cool)	339 – 10^9 photon counts/s (Uncool)[39]
Readout noise	+/- 1mV offset + 0.5mV ripple noise[40]	n/a	~0
Spectral response	230-700, peak at 400	n/a	350-900, peak at 480

We have also demonstrated the use of SPCImager for characterisation of OLED pixel arrays for both steady state measurement and fast transient measurement. The SPCImager is capable of observing dynamic behaviour of the OLED pixel overshoot occurring over a very short time scale which is inaccessible to most sCMOS and CCD sensors. Each SPCImager SPAD pixel can achieve 10^7 photon counts per second for 100ns exposure, and dark count as low as 4 counts/s when cooled. Also, neutral density (ND) filters can be applied to extend the dynamic range. Table 4-2 shows an outline comparison of the SPAD-based SPCImager and other state-of-the-art systems. SPCImager measures significantly faster and is capable of nonuniformity measurement.

[39] 64 SPADs are activated out of the 1024 SPADs on the array.
[40] ADC noise is not applicable. Maximum output signal voltage: 4V.

Table 4-2 Performance Comparison of SPCImager with existing imager sensor based systems

Measurement system	2-in-1 Imaging Colorimeter [241]	MotionMaster [242]	SPCImager (this work)
Image sensor technology	CMOS	CCD	SPAD
Frame time	0.5s	typ. 0.26ms – 0.52ms	< 100 μs (> 10 kHz)
Dynamic range	0.01 cd/m2 – 5000 cd/m2[41]	n/a	4 – 10^7 photon counts/s (aprox. 2×10-4 – 550 cd/m2 at 520 nm) for 100ns exposure to 1s exposure, -5C° cooled
Resolution	1900 × 1180	n/a	320 × 240
Noise level	1.2 % – 3.5 %, depends on luminance scale	n/a	~0 readout noise, ~30 dB SNR for QIS modelled signal

[41] ND filter is applied for 1000 cd/m^2 luminance.

5 Summary and conclusions, Future Work and Outlook

This chapter summarises the work described in this thesis outlining the key research objectives, the research undertaken to achieve them and the conclusions. The future tasks are listed which is needed to complete this work to achieve a high impact value. Finally, an outlook to future microdisplays, pixels, OLEDs and characterisation tools is given.

5.1 Summary and conclusions

This thesis aims at exploring the development of high-performance tandem structure OLED microdisplay pixel and its characterisation. The pixel design is targeting to deliver high dynamic range to drive the TOLED which is expected with a double current efficiency. In the meanwhile, the pixel is required to have a small pixel pitch, minimal connectivity and low power consumption to be integrated on a scalable microdisplay pixel array.

Chapter 2 shows the development of the first-ever TOLED SPICE model which offers high accuracy simulation to the electrical response. The dual loop model emulates the structure of a TOLED. The model is verified over fitting of multiple TOLEDs with the same material to illustrate the OLED manufacturing process variation. Moreover, it is also employed for parameter extraction of multiple TOLEDs with different OLED layer material to investigate the effect of different materials on the electrical characteristics. And hence, it is useful to the research and development of high-performance tandem OLED stacks.

TOLED has a doubled current efficiency compared to single-unit OLEDs. However, the high current efficiency comes at a price of s doubled drive voltage. The microdisplay pixel needs to achieve a high voltage output and high dynamic range. To address these challenges, several microdisplay pixels are designed and implemented in Chapter 3. An annular shape MOSFET is employed to demonstrate low leakage and high input dynamic range pixels. In addition, an analogue PWM pixel is designed. This pixel achieved the pulse-width in-pixel generation without any bias current at a sub-pixel pitch of 5×5 μm^2. It allows a full voltage dynamic range (0 to VDD) for the drive of OLED anode. The analogue pixel realises less 1% linearity and 2% variation in a 4×12 test array. Compared to the previous published analogue PWM pixel (Blalock pixel [6]), the novel design is with less power consumption and smaller pixel pitch (12 µm for Blalock pixel).

Nevertheless, improvements are still needed for the implementation in large microdisplay arrays. First, care must be taken to the routing, buffering of the Ramp signal. The pulse-width generation is highly sensitive to the ramp signal. The RC decay along the ramp wire track or other electrical noise (such as power noise, kT/C, clock coupling) would have effects on the OLED output. Second, the MOSFET sizing and layout need to be improved, as the variation level is expected to be worse over a larger silicon area.

Electrical characterisation results of the test pixels shown in Chapter 3 is susceptible to the electrical interference of the measurement setup. As the OLED pixel is small, the anode output is sensitive to any additional parasitic resistance and capacitance. Therefore, the optical measurement would be required to characterise the pixels.

While the conventional light measurement instruments such as PMT, CCD and CMOS are proven in terms of measuring mainstream electronic displays. As OLED microdisplays evolve to high dynamic range, ultra-fast switching and small pixel pitch, the optical characterisation in pixel level also expects more advance measurement devices. CMOS SPAD sensors have the distinct advantage of single photon sensitivity and picosecond time resolution. It is an emerging technology for light measurements.

In chapter 4, two CMOS SPAD sensors are demonstrated for characterisation of the TOLED test pixel. The reconfigurable single point sensor-FlashTDC allows a high dynamic range of photon count and a fast sampling rate up to 188 kHz which outperforms some PMTs [182]. It is employed for the 2T pixel flicker optical measurements. The results show in agreement with simulation TOLED current response without any electrical interference as presented in chapter 3. The other more impressive CMOS SPAD imager is the SPCImager. Although there is only 1-bit depth in each pixel, it achieves a very high frame rate with low dark count and ~0 readout noise. The theoretical QIS model is verified in experiments to give a high dynamic range measurement through oversampling the bit-planes. Both high dynamic range steady-state and transient dynamic behaviour has been measured. Moreover, microsecond OLED turn-on overshoot behaviour is observed. It is the first time the transient overshoot behaviour is observed by an image sensor instead of single point sensors [236-238]. The sensor is capable of measuring fast transient behaviour over the pixels in the field of view to quantify variations.

However, due to the instability of the optical setup, it is difficult to find the focus and field of view for the single-point sensor-FlashTDC. The similar situation also happens to SPCImager. The measurement results could be affected as the pixels move out of focus.

5.2 Contribution to knowledge

Four key contributions to knowledge are discussed here:

1. A novel SPICE equivalent circuit model for the description of TOLED electrical characteristics has been developed. The model is based on the conventional single – unit OLED SPICE models and its tandem stack structure. The model is verified to achieve high accuracy over a wide voltage and current dynamic range.
2. The use of an annular transistor in-pixel has been demonstrated to realise low leakage sample-and-hold circuit for a conventional 2T pixel. The annular transistor pixel has been measured to achieve less than 16% flicker over 40ms without any reverse bias.

3. A high dynamic range pixel based on an analogue PWM approach has been developed. The 6T analogue pixel generates pulse-width modulation in-pixel. It takes advantage of the full voltage swing of the thick oxide transistors to achieve a high voltage dynamic range. A small test array (4×12) featuring 5μm analogue PWM pixel has been implemented with white tandem OLED and characterised optically with a CMOS SPAD imager.
4. The use of CMOS SPAD sensors for optical measurement and characterisation of the OLED test pixels has been demonstrated. Both single point and image array SPAD sensors are employed. These measurements are the first applications of SPAD sensors for OLED microdisplay optical measurements. The CMOS SPAD sensors are capable of capturing dynamic behaviour occurring over a short time scale (10 μs). The measurements can be extended to a broader range of displays and relevant photonic technologies.

5.3 Future work

5.3.1 Analogue PWM pixel

The analogue PWM pixel conceived in this thesis still requires some work to be done for them to be scalable for the development of larger microdisplay arrays. First, the pixel's optical characterization is not yet fulfilled with the SPCImager. The pixel setting has to be simplified (in PCM mode rather than PWM mode) due to the unreliable optical measurement setup. The non-linearity and variation can be measured optically without any electrical interference. And the optical measurement can cover the full 4×12 array.

Second, further modifications in the layout design and MOSFET sizing can be applied to improve the uniformity. The buffer and routing of the Ramp signal are also critical which could reduce the variation over different rows of pixels.

5.3.2 CMOS SPAD measurement

The optical setup for the CMOS SPAD sensors needs to be optimised such that it does not affect the measurement data validity. Due to the constraint of the optical setup, the focus between the sensor and the test pixel devices would influence the repeatability and accuracy of the measurement results. Microscopes with higher magnification, and more compact and finer focus setting would facilitate the measurement.

5.4 Future Outlook

Over the past decade, OLED technology has shown great potential in commercial display applications such as mobile phone displays, TVs. It starts to gain market share from the long-time domineer LC for its characteristics including wide viewing angle, low power consumption, high contrast ratio, good

colour performance and fast switching. OLED microdisplay, in combination with CMOS integration, is able to achieve high speed and low power. It is an ideal device for NTE applications, such as AR, VR which is imminent for the future 5G, IoT (Internet of things) systems.

5.4.1 OLED device

The use of direct patterning and tandem structure OLED could be a game changer for developing high luminous OLED device. In theory, with both technology implemented the luminance should become × 6 with the same current density. Tandem OLED has already been reported in commercial OLED displays development [67-69, 243, 244]. The main advantage is to extend the lifetime of OLED displays for general applications, e. g. TVs.

On the other hand, the colour direct patterning has been demonstrated in OLED microdisplays. eMagin has commercialised its direct patterning OLED microdisplay [44], although it is not yet available to general customers. It can be seen that commercialisation of OLED devices that feature both tandem and direct patterning are commercialized in the near future. OLED would become dominant in NTE application microdisplays.

5.4.2 Microdisplays

Although OLED microdisplays are becoming popular, the other microdisplay technology, such as LCoS, DMD would still maintain the mainstream projector market, thanks to their extremely high level of luminance and long lifetime.

The forthcoming LED microdisplay could be a threat to OLED as the high luminance and long lifetime provided by inorganic LEDs. Some work[245] has already begun in this area. However, it is still a long way for the commercialisation of microLED displays.

5.4.3 SPAD sensors for light measurement

When set beside the other technologies such as CCD and CMOS, CMOS SPAD is a relatively young technology. The commercial potential across a broad and diverse range of applications from medical imaging to automotive LIDAR means that CMOS SPAD sensors and arrays are currently the focus of a great deal of research and development effort in both technology and design and are expected to remain so for some years to come. One recent *technology* trend that illustrates this is the development of SPAD-optimized CMOS processes, from Back Side Illuminated (BSI) [202] to 3D stacking [224]. This means that the rate of performance improvement in CMOS SPADs is currently very high and is further enhanced by design because Application Specific SPAD ICs – optimally designed for a given application – are readily achievable. Thus, we can look forward to continuing rapid performance improvement in CMOS SPAD arrays that is likely to outpace improvements in the rival technologies.

6 Appendices

There are other pixel circuit trial apart from the ones (the annular two-T SF pixel and analogue PWM pixel) that are present in the chapter 3. This supplementary chapter introduces a couple of pixels that the author explored and implemented in the TOLED test pixel tape-out. The pixel circuit operation and basic measurement result will be discussed.

6.1 All NMOS PWM pixel

The pixel circuit schematic is shown in Figure 6-1. Similar to the analogue PWM pixel presented in Figure 3-20, the pixel generates pulse by comparing the V_C storing in the pixel MOS capacitor and a global ramp signal. By switching charges on node V_G, V_D is switching from ON to OFF. The difference is the pixel circuit is composed only by four NMOS transistors and one NMOS capacitor. The benefit of elimination of the PMOS is the possibility to further reduce pixel pitch. As the pixel only employs NMOS transistors, there is no need to create NWELL inside the pixel. Table 6-1 shows the transistor sizing after Monte Carlo simulations to verify the pixel performance. Figure 6-2 shows the 2×2 all NMOS PWM pixel layout, they are arranged in a common centroid manner to reduce pixel-to-pixel variations and size of the pixel. The pixel circuit achieved a 4.7 µm pixel pitch.

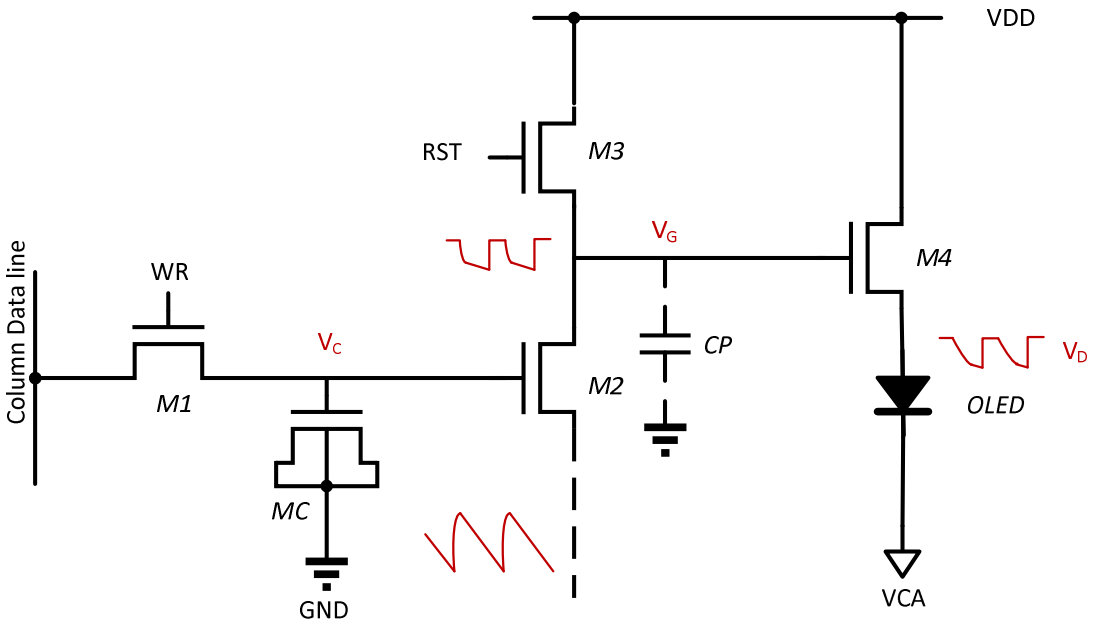


Figure 6-1 schematic of the all NMOS variation of the analogue PWM pixel

Table 6-1 All NMOS PWM pixel transistors' size

Transistor	Description	Width (µm)	Length (µm)
M1	DATA input/WR	0.5	0.5
M2	Comparator transistor	1.18	1.08
M3	Reset/V_G pull up	0.5	0.5
M4	Output drive transistor	3	0.5
MC	Storage MOS cap	3.62	1.68

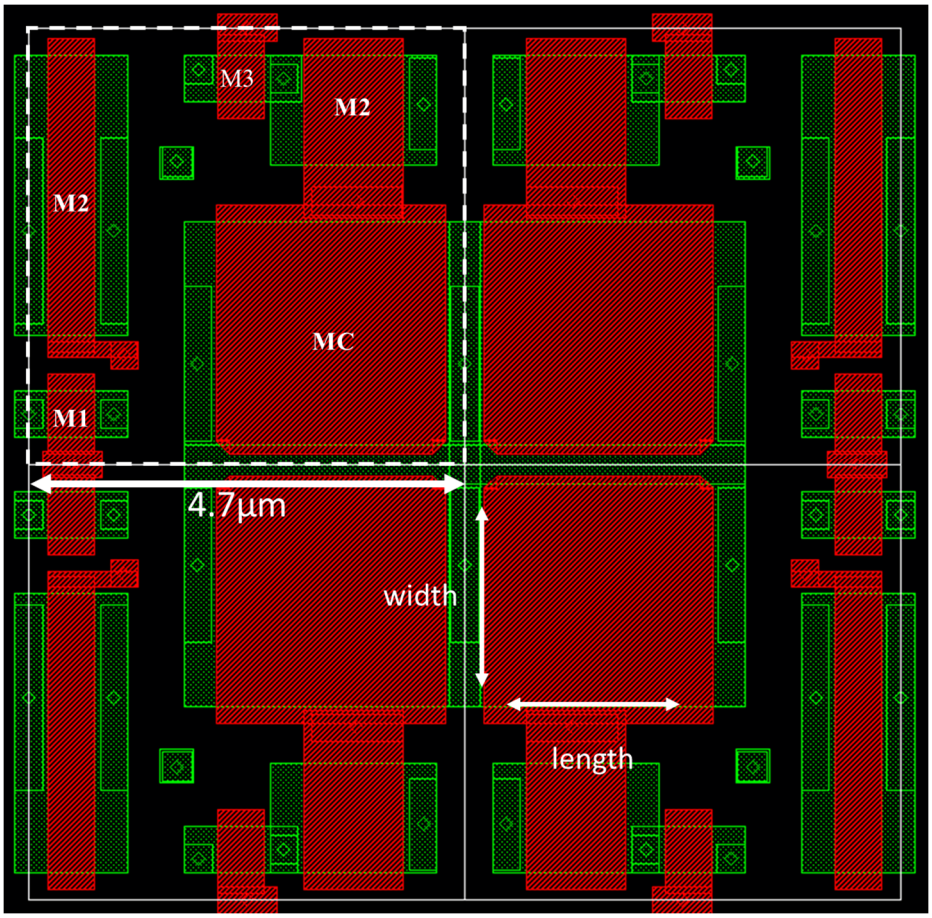
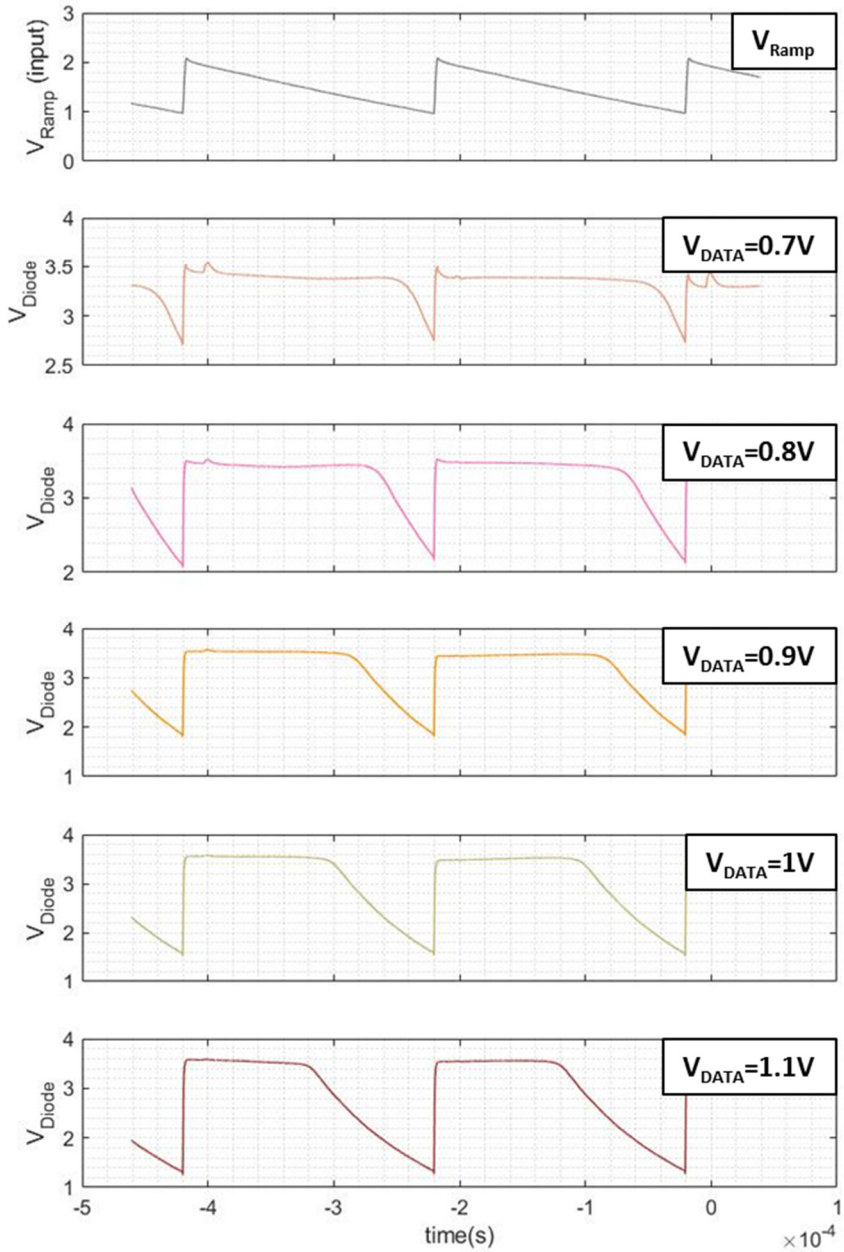


Figure 6-2 The all NMOS PWM pixel layout

The measured input Ramp signal and the electrical output from the OLED anode is shown in Figure 6-3. The response of the V_{diode} scales down with increasing V_{DATA}. However, there is two inherent flaws with the pixel circuit. First, V_{diode} is switched at a slow slew rate, which depends on the mobility of M2. The variation of M2 would impact the output nonuniformity. Second, V_{diode} cannot be switched off completely, as shown for V_{DATA}=1.6V, V_{diode} switch from high to low when the cycle starts. Thus, the pixel is not presented as the main contribution, but it is still worth to explore for its small pixel pitch.



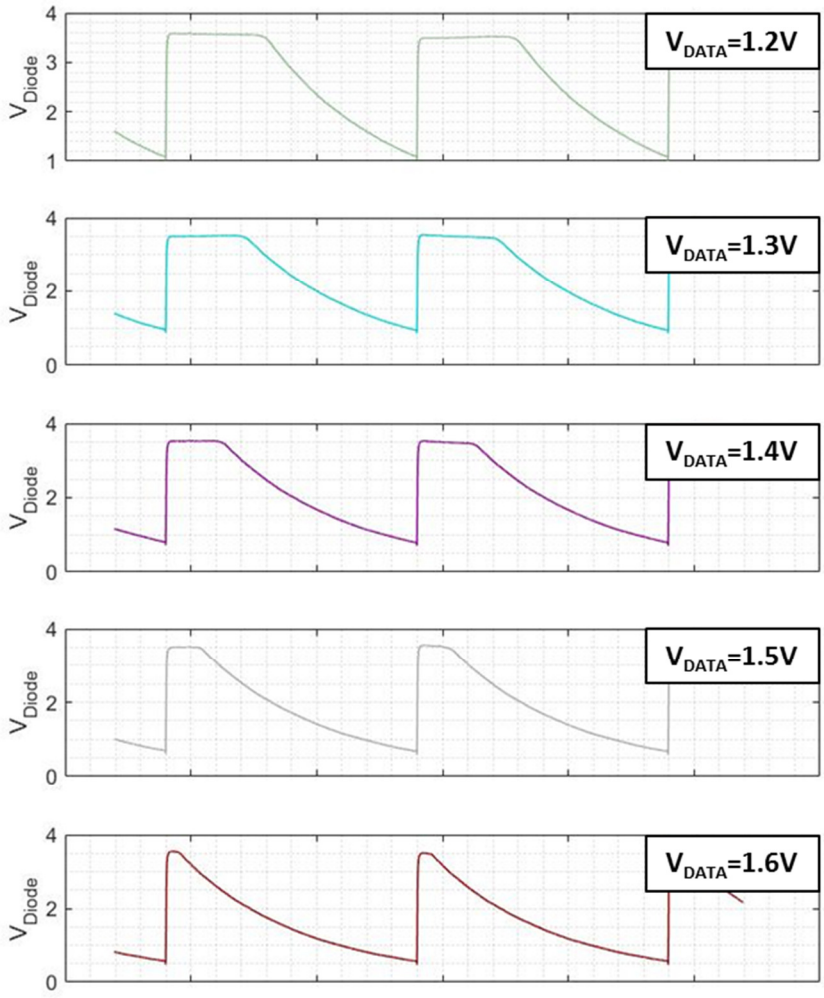


Figure 6-3 Measured Ramp signal and anode output response, V_{DATA} input as 0.7 V to 1.6 V with 0.1 V step.

6.2 Thyristor structure PWM pixel

Another pixel circuit that has been implemented is the adapted analogue PWM pixel with a thyristor structure output. The pixel circuit is shown in Figure 6-4. The main difference is the extra transistor MN3 (highlighted in the figure). The aim is to increase the output slew rate by the positive feedback introduced by MN3. The sizing of the transistors is similar to the analogue PWM pixel, as shown in Table 6-2. Due to the extra NMOS transistor, the pixel pitch increases from 5 µm to 5.25 µm. The 2×2 pixel layout is shown in Figure 6-5.

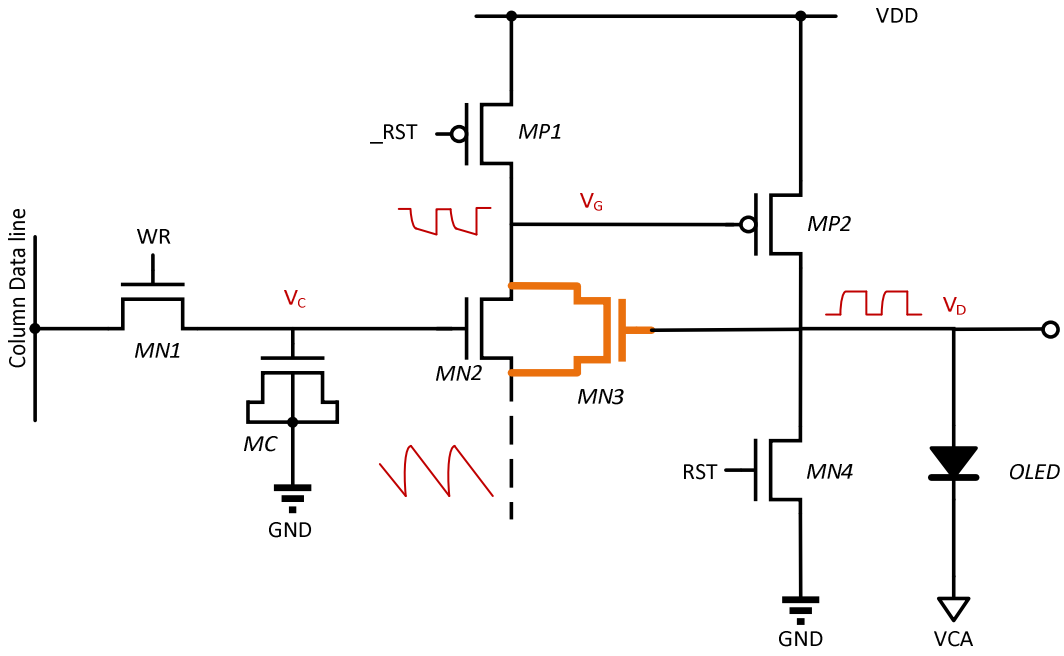


Figure 6-4 schematic of the analogue PWM pixel with thyristor

Table 6-2 Thyristor PWM pixel transistors' size

Transistor	Description	Width (µm)	Length (µm)
MN1	DATA input/WR	0.5	0.5
MN2	Comparator transistor	1.05	1.32
MN3	Thyristor NMOS	0.5	0.5
MN4	Reset/Output pull down	0.5	0.5
MP1	Reset/V_G pull up	0.5	0.5
MP2	Output drive transistor /Thyristor PMOS	0.5	0.67
MC	Storage MOS cap	3.83	1.24

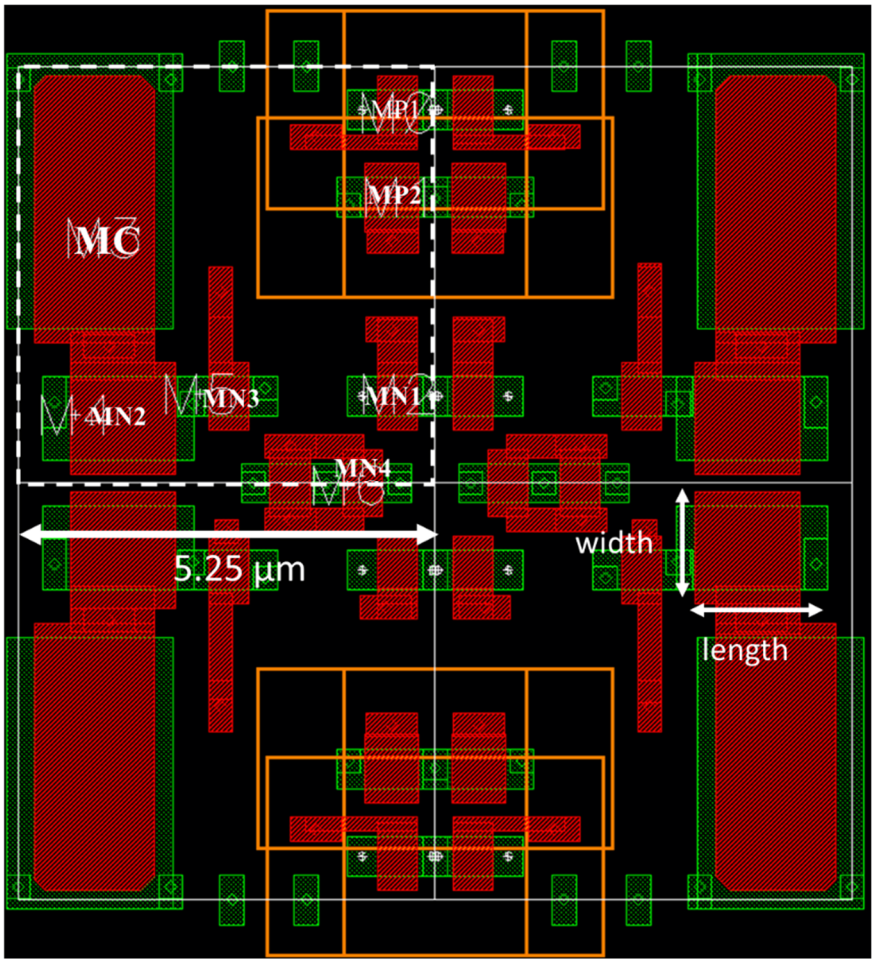
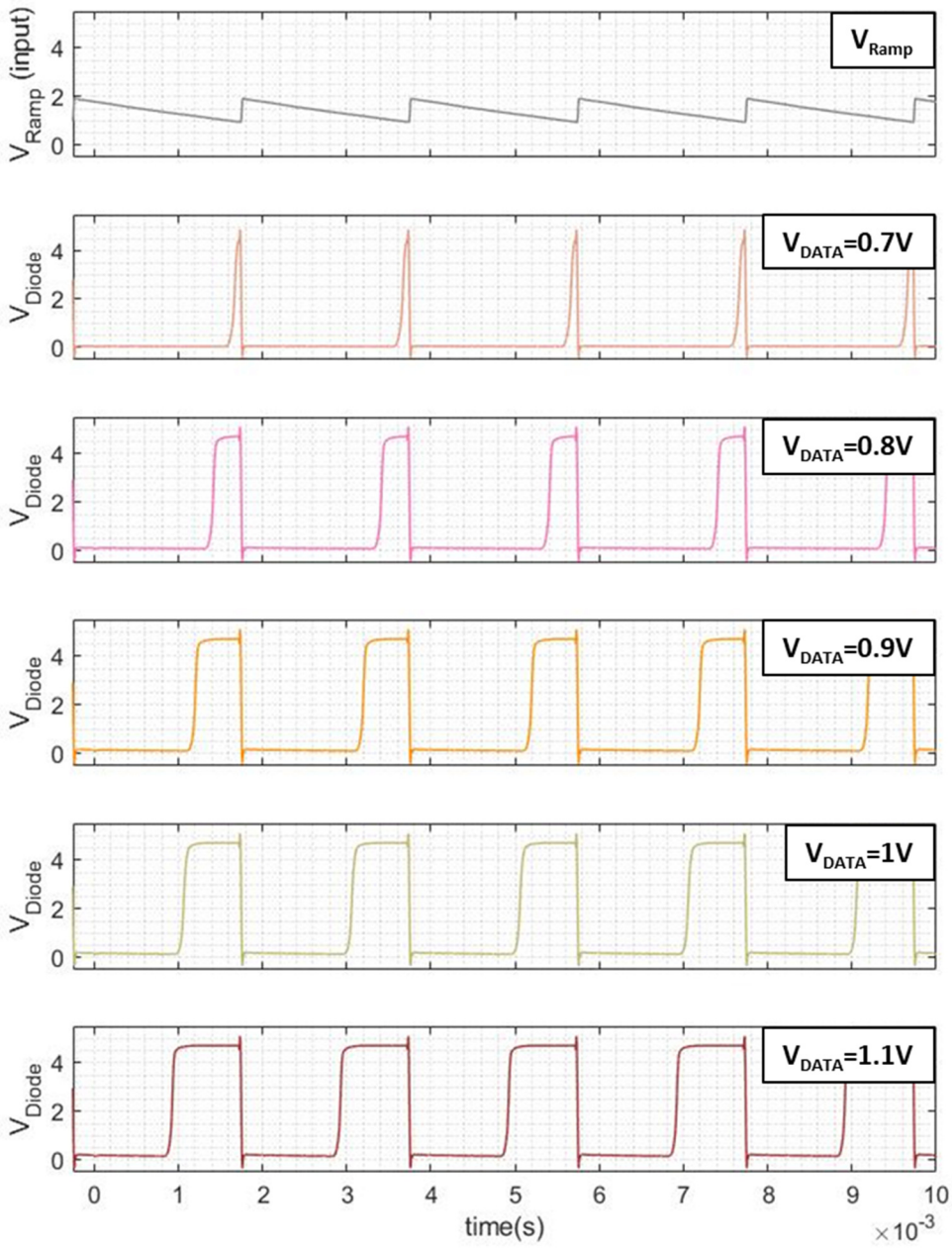


Figure 6-5 The thyristor PWM pixel layout

The Ramp signal and the measured anode node voltage output V_{diode} is shown in Figure 6-6. The slew is faster compared to Figure 3-40. However, there is a charge injection on node V_G (in Figure 6-4) through the drain-source channel. The V_{diode} does not start from 0V, especially for higher V_{DATA}. It is not obvious for V_{DATA}=0.7V, but the leakage is shown for other DATA voltages.



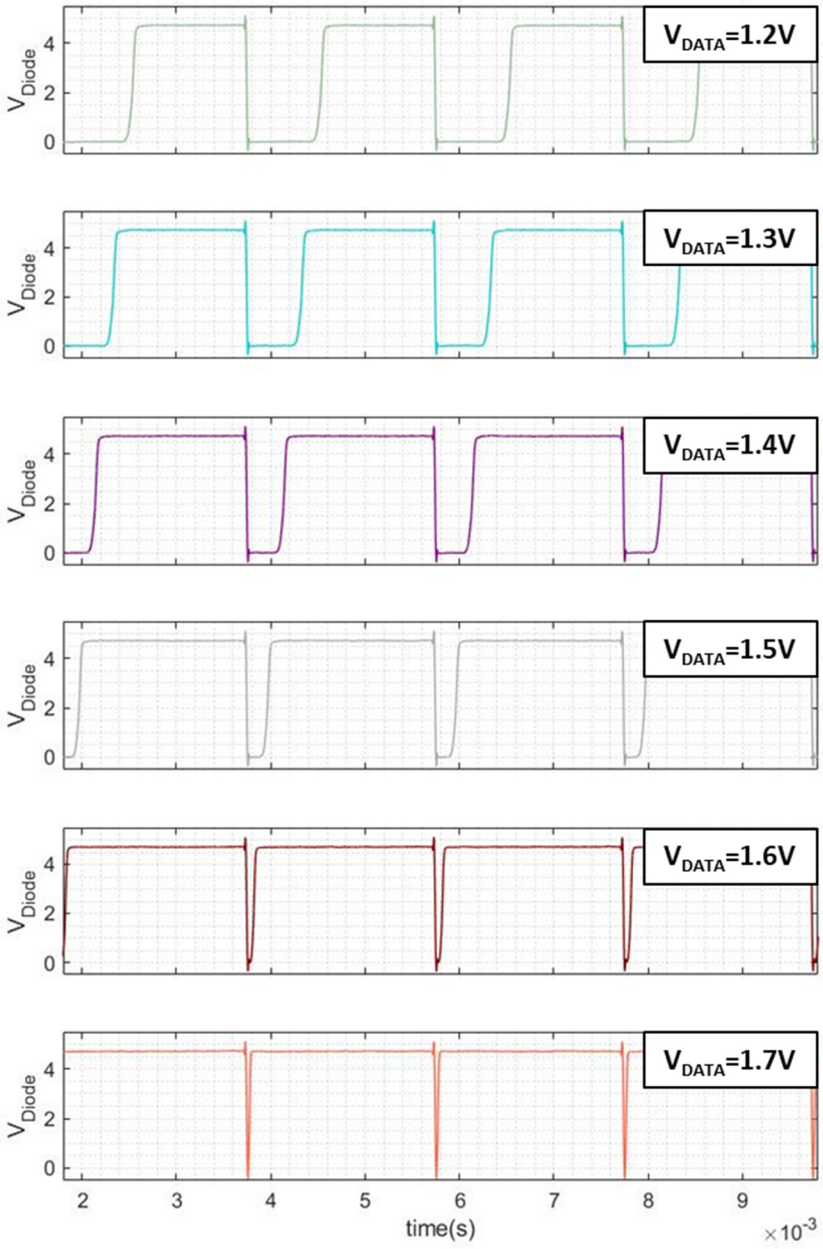


Figure 6-6 Measured Ramp signal and anode output response, V_{DATA} input as 0.7 V to 1.7 V with 0.1 V step.

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